
ARM®-based 32-bit MCU, up to 32KB Flash, 8 timers, ADC & comm. interfaces, 1.8-5.5V

Features

- ARM® 32-bit Cortex-M0 CPU, frequency up to 48 MHz
- Memories
 - ◇ 16/32KB of Flash memory
 - ◇ 4 KB SRAM
- CRC calculation unit
- Reset and power management
 - ◇ Digital and I/Os supply: VDD = 1.8 - 5.5V
 - ◇ Analog supply: VDDA = 1.8 - 5.5V
 - ◇ Power-on/Power down reset(POR/PDR)
 - ◇ Programmable voltage detector(PVD)
 - ◇ Low power modes: Sleep, Stop, Standby
- Clock management
 - ◇ 4 to 24 MHz crystal oscillator
 - ◇ 32 kHz oscillator for RTC with calibration
 - ◇ Internal 8 MHz RC oscillator
 - ◇ Internal 40 kHz RC oscillator
 - ◇ PLL use for CPU clock
- Up to 39 fast I/Os
 - ◇ All mappable on external interrupt vectors
 - ◇ With 5V tolerant capability when power supply is 3V
- DMA controller
 - ◇ 5 channel
 - ◇ Support peripherals: TIMER/ADC/SPI/I²C/USART
- One 12-bit, 1.0 us ADC(up to 10 channels)
 - ◇ Conversion range: 0 to 5.5 V
 - ◇ Embedded temp sensor
- 9 timers
 - ◇ One 16-bit advanced-control timer for six channel PWM output
 - ◇ Fix 16-bit timers, with up to four IC/OC,OCN, usable for IR control decoding
 - ◇ Independent and system watchdog timers
 - ◇ SysTick timer
- Communication interfaces
 - ◇ One I²C interface supporting Fast Mode Plus(1Mbit/s) with 20mA current sink, SMBus/PMBus and wakeup
 - ◇ One USARTs supporting master synchronous SPI and modem control, one with ISO7816 interface LIN, IrDA, auto baud rate detection and wakeup feature
 - ◇ Two SPIs(24 Mbit/s) with 4 to 16 programmable bit frames, one with I²S interface multiplexed
- HDMI CEC, wakeup on header reception
- Debug mode
 - ◇ Serial wire debug(SWD)
- 96-bit unique ID

- Packages
 - ✧ TSSOP20
 - ✧ UFQFPN28 4x4 mm
 - ✧ UFQFPN32 5x5 mm
 - ✧ LQFP32 7x7 mm
 - ✧ LQFP48 7x7 mm

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1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the FCM32F042x microcontrollers.

For information on the arm Cortex-M0 core, please refer to the Cortex-M0 Technical Reference Manual, available from the www.arm.com website.



2 Description

The FCM32x031x microcontrollers incorporate the high-performance arm Cortex-M0 32-bit RISC core operating at up to 48 MHz frequency, high-speed embedded memories (up to 32 Kbytes of Flash memory and 8 Kbytes of SRAM), and an extensive range of enhanced peripherals and I/Os. All devices offer standard communication interfaces (I²C, SPI/I²S, USART and HDMI-CEC), 12-bit ADC, four general purpose 16-bit timers, one general purpose 32-bit timer and an 16-bit advanced-control PWM timer.

The FCM32x031x microcontrollers operate in the -40 to +85C and -40 to +105C temperature ranges, from a 1.8 to 5.5 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

The FCM32x031x microcontrollers include devices in several different packages ranging from 20 pins to 48 pins with a die form also available upon request. Depending on the device chosen, different sets of peripherals are included.

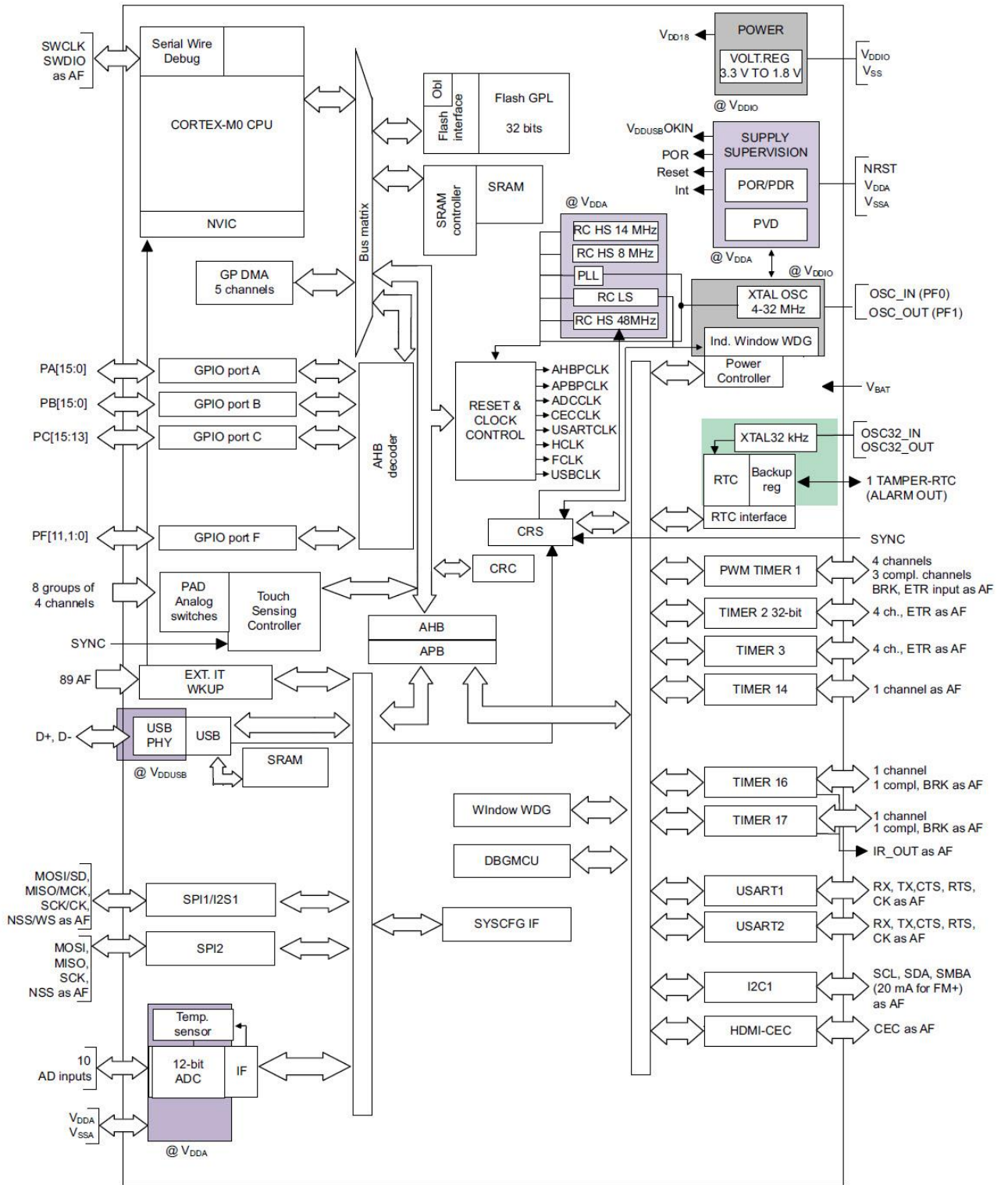
These features make the FCM32x031x microcontrollers suitable for a wide range of applications such as application control and user interfaces, hand-held equipment, A/V receivers and digital TV, PC peripherals, gaming and GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms and HVACs.

FCM32x031x medium-density device features and peripheral counts

Peripheral		FCM32F031Fx		FCM32F031Gx		FCM32F031Kx		FCM32F031Cx	
Flash(Kbytes)		16	32	16	32	16	32	16	32
SRAM(Kbytes)		4							
Timers	Advanced control	1 (16-bit)							
	General purpose	4 (16-bit)							
Comm. interfaces	SPI/I ² S ⁽¹⁾	1/1		1/1		1/1		2/2	
	I ² C	1							
	USART	1							
	CAN	0							
	CEC	0							
12-bit ADC (number of channels)		1 (11)		1 (12)					
GPIOs		15		23		25(LQFP32) 27(UFQFPN32)		39	
Max. CPU frequency		48 MHz							
Flash Turbo		-							
Operating voltage		1.8~5.5V							
Operating temperature		-40~85							
Packages		TSSOP20		UFQFPN28		LQFP32 UFQFPN32		LQFP48	

1. SPI/I²S interfaces can be used either in SPI mode or in I²S audio mode

Block diagram



3 Functional overview

3.1 ARM® Cortex-M0 core

ARM® Cortex-M0 is a generation of arm 32-bit RISC processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM® Cortex-M0 processors feature exceptional code-efficiency, delivering the high performance expected from an arm core, with memory sizes usually associated with 8- and 16-bit devices.

3.2 Memories

The device has the following features:

- 4/8 KB of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states
- The non-volatile memory is divided into two arrays:
 - 16/32 KB of embedded Flash memory for programs and data
 - Option Bytes

The option bytes are used to write-protect the memory (with 4 KB granularity) and/or readout-protect the whole memory with the following options:

- Level 0: no readout protection
- Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
- Level 2: chip readout protection, debug features(SWD) and boot in RAM selection disabled

3.3 Boot modes

At startup, the boot pin and boot selector option bits are used to select one of the three boot options:

- Boot from User Flash memory
- Boot from System Memory
- Boot from embedded SRAM

The boot pin is shared with the standard GPIO and can be disabled through the boot selector option bits. The boot loader is located in System Memory.

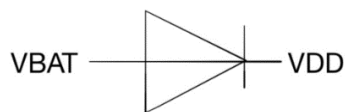
3.4 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a CRC-32 (Ethernet) polynomial.

3.5 Power management

3.5.1 Power supply

- VDD = 1.8 - 5.5V: external power supply for I/Os and the internal regulator. It is provided externally through VDD pins.
- VDDA = 1.8 - 5.5V: external analog power supply for ADC, Reset blocks, RCs and PLL. It is provided externally through VDDA pin. The VDDA voltage level must be always greater or equal to the VDD voltage level and must be established first.
- VBAT = 1.8 – 5.5V: The other optional power supply. Power supply for VDD (through internal DIODE) when VDD is not present.



3.5.2 Power supply supervisors

The device has integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 1.8 V. The device remains in reset mode when the monitored supply voltage is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

- The POR monitors only the VDD supply voltage. During the startup phase it is required that VDDA should arrive first and be greater than or equal to VDD.
- The PDR monitors both the VDD and VDDA supply voltages, however the VDDA power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that VDDA is higher than or equal to VDD.

The device features an embedded programmable voltage detector (PVD) that monitors the VDD power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when VDD drops below the V_{PVD} threshold and/or when VDD is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.5.3 Voltage regulator

The regulator has two operating modes and it is always enabled after reset.

- Main (MR) is used in normal operating mode (RUN)
- Low power (LPR) can be used in Stop mode where the power demand is reduced.

In Standby mode, it is put in LPR mode. In this mode, MCU core and SRAM, SFRs and most peripherals stopped, the contents of the registers and SRAM are not lost.

3.5.4 Low-power modes

The FCM32x031x microcontrollers support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**
In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- **Stop mode**
Stop mode achieves very low power consumption while retaining the content of SRAM and registers. All clocks in the 1.5 V domain are stopped, the PLL, the HIS RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode. The device can be woken up from Stop mode by any of the EXTI lines. The EXTI line source can be one of the 16 external lines, the PVD output, RTC, I2C1, USART1, USB or the CEC. The CEC, USART1 and I2C1 peripherals can be configured to enable the HIS RC oscillator so as to get clock for processing incoming data. If this is used when the voltage regulator is put in low power mode, the regulator is first switched to normal mode before the clock is provided to the given peripheral.
- **Standby mode**
[The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator enter LPR mode. PLL, the HIS RC and the HSE crystal oscillators are also switched off. The content of SRAM and registers are retained.](#)
The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pins, or an RTC event occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

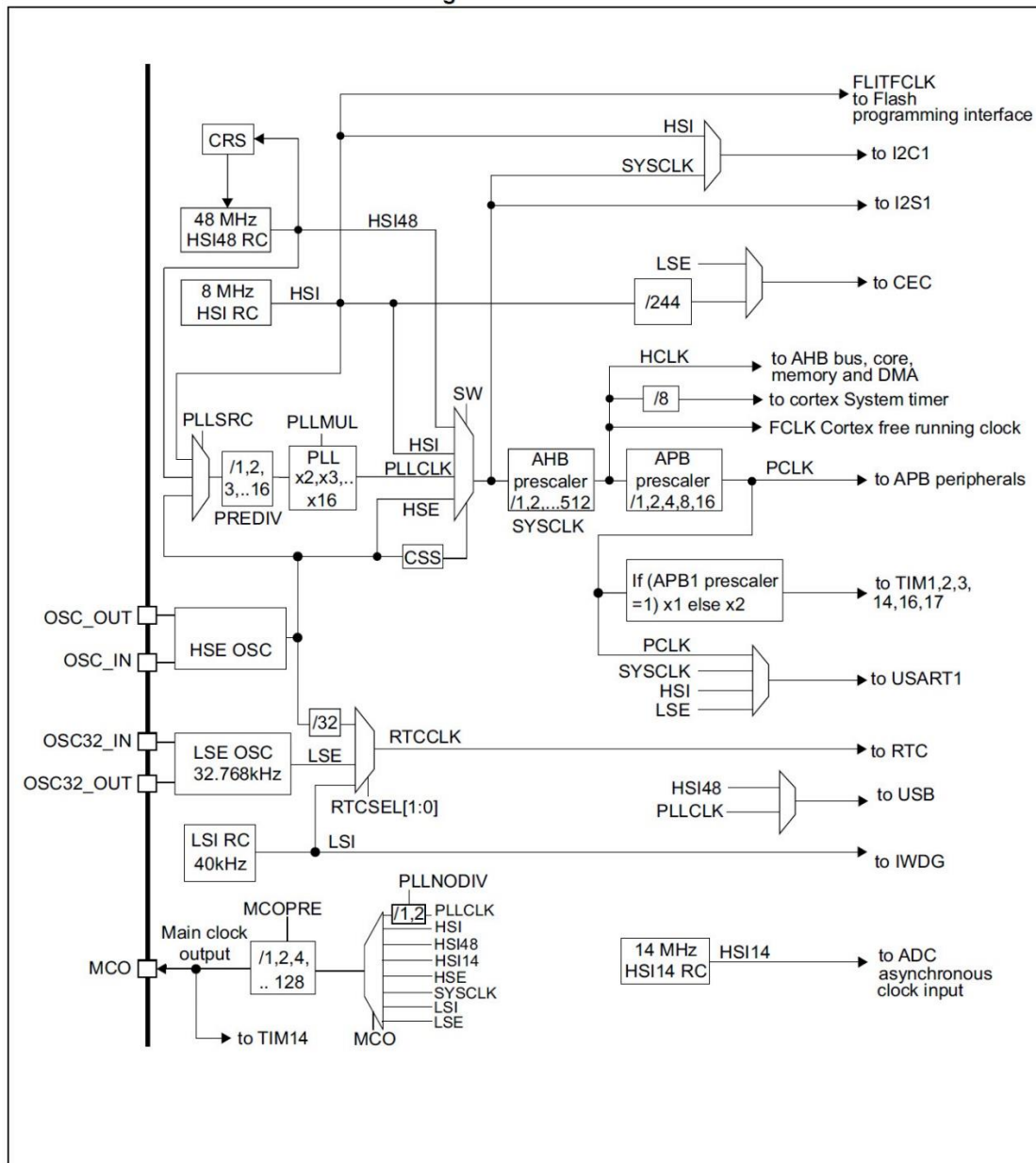
3.6 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary.

Several prescalers allow the application to configure the frequency of the AHB and the APB domains. The maximum frequency of the AHB and APB domains is 48 MHz.

Additionally, also the internal RC 48 MHz oscillator can be selected for system clock or PLL input source. This oscillator can be automatically fine-trimmed by the means of the CRS peripheral using the external synchronization.

Clock tree



3.7 GPIO

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

The I/O configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.8 Direct memory access controller (DMA)

The 5-channel general-purpose DMAs manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers.

The DMA supports circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

DMA can be used with the main peripherals: SPIx, I2Sx, I2Cx, USARTx, all TIMx timers (except TIM14) and ADC.

3.9 Interrupts and events

3.9.1 Nested vectored interrupt controller (NVIC)

The FCM32x031x family embeds a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels (not including the 16 interrupt lines of Cortex-M0) and 4 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved

3.9.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 24 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 38 GPIOs can be connected to the 16 external lines.

3.10 Analog-to-digital converter (ADC)

The 12-bit analog-to-digital converter has up to 10 external and 3 internal (temperature sensor, voltage reference, VBAT voltage measurement) channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

3.10.1 Temperature sensor (TS)

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

3.10.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC. V_{REFINT} is internally connected to the ADC_IN17 input channel.

3.10.3 V_{BAT} battery voltage monitoring

The embedded hardware feature allows the application to measure the VBAT battery voltage using the internal ADC channel ADC_IN18. As the VBAT voltage may be higher than VDDA, and thus outside the ADC input range, the VBAT pin is internally connected to a bridge divider by 2. As a consequence, the converted digital value is half of the VBAT voltage.

3.11 Timers and watchdogs

The FCM32x031x devices include up to five general-purpose timers and an advanced control timer.

Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	CCP channels	Complementary outputs
Advanced control	TIM1	16-bit	Up, down, Up/down	1~65536	Yes	4	Yes
General purpose	TIM2	32-bit	Up, down, Up/down	1~65536	Yes	4	No
	TIM3	16-bit	Up, down, Up/down	1~65536	Yes	4	No
	TIM14	16-bit	Up	1~65536	No	1	No
	TIM16, TIM17	16-bit	Up	1~65536	Yes	1	Yes

3.11.1 Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on six channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can work also in debug mode.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers via the Timer Link feature for synchronization of event chaining.

3.11.2 General-purpose timers (TIM2/3/14/16/17)

There are five synchronizable general-purpose timers embedded in the FCM32x031x devices. Each general-purpose timer can be used to generate PWM outputs, or as simple time base.

TIM2/3

FCM32x031x devices feature two synchronizable 4-channel general-purpose timers. TIM2 is based on a 32-bit auto-reload up/down counter and a 16-bit prescaler. TIM3 is based on 1 16-bit auto-reload up/down counter and a 16-bit prescaler. They feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.

The TIM2 and TIM3 general-purpose timers can work together or with the TIM1 advanced-control timer via the Timer Link feature for synchronization of event chaining.

TIM2 and TIM3 both have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Their counters can be frozen in debug mode.

TIM14

This timer is based on a 16-bit auto-reload up counter and a 16-bit prescaler.

TIM14 features one single channel for input capture/output compare, PWM or one-pulse mode output. Its counter can be frozen in debug mode.

TIM16/17

Both timers are based on a 16-bit auto-reload up counter and a 16-bit prescaler.

They each have a single channel for input capture/output compare, PWM or one-pulse mode output.

They have a complementary output with dead-time generation and independent DMA request

generation.

Their counters can be frozen in debug mode.

3.11.3 Independent watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 12-bit down counter with user-defined refresh window. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.11.4 System window watchdog (WWDG)

The system window watchdog is based on a 7-bit down counter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PLCLK). It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.11.5 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter.

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source (HCLK or HCLK/8)

3.12 Real-time clock (RTC) and backup registers

The backup registers are five 32-bit registers used to store 20 bytes of user application data. They are not reset by a system or power reset, or at wake up from Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

- Calendar with subseconds, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- Automatic correction for 28, 29 (leap year), 30, and 31 day of the month
- Programmable alarm with wakeup from Stop and Standby mode capability
- On-the-fly correction from 1 to 32767 RTC cloc pulses. This can be used to synchronize the RTC with a master clock
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy

- Two anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision

The RTC clock sources can be:

- A 32768 Hz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32

3.13 Inter-integrated circuit interface (I²C)

The I²C interface can operate in multimaster or slave modes. It can support Standard mode (up to 100 kbit/s), Fast mode (up to 400 kbit/s) and Fast Mode Plus (up to 1Mbit/s) with 20mA output drive.

They supports 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (two addresses, one with configurable mask). It also includes programmable analog and digital noise filters.

In addition, I2C1 provides hardware support for SMBUS 2.0 and PMBUS 1.1. It also has a clock domain independent from the CPU clock, allowing the I²C1 to wake up the MCU from Stop mode on address match.

The I2C peripherals can be served by the DMA controller.

FCM32x031x I²C implementation

I ² C features	I ² C1
7-bit addressing mode	Y
10-bit addressing mode	Y
Standard mode (up to 100 kbit/s)	Y
Fast mode (up to 400 kbit/s)	Y
Fast Mode Plus with 20mA output drive I/Os (up to 1Mbit/s)	Y
Independent clock	Y
SMBus	Y
Wakeup from STOP	Y

3.14 Universal synchronous / asynchronous receiver / transmitter (USART)

The device embeds two universal synchronous/asynchronous receivers/transmitters (USART1, USART2) which communicate at speeds up to 12.5 Mbit/s.

They provide hardware management of the CTS, RTS and RS485 DE signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. USART1 supports also SmartCard communication (ISO7816), IrDA SIR ENDEC, LIN Master/Slave capability and auto baud rate feature, and has a clock domain independent to the CPU clock, allowing to wake up the MCU from Stop mode.

The USART interfaces can be served by the DMA controller.

•

FCM32x031x USART implementation

USART modes/ features	USART1
Hardware flow control for modem	Y
Continuous communication using DMA	Y
Multiprocessor communication	Y
Synchronous mode	Y
Smartcard mode	Y
Single-wire half-duplex communication	Y
IrDA SIR ENDEC block	Y
LIN mode	Y
Dual clock domain and wakeup from Stop mode	Y
Receiver timeout interrupt	Y
Modbus communication	Y
Auto baud rate detection	Y
Driver Enable	Y

3.15 Serial peripheral interface (SPI) / Inter-integrated sound interface (I²S)

One standard I²S interface (multiplexed with SPI) supporting four different audio standards can operate as master or slave at half-duplex communication mode. It can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by an 8-bit programmable linear prescaler. When operating in master mode, it can output a clock for an external audio component at 256 times the sampling frequency.

FCM32x031x SPI/I²S implementation

SPI features	SPI1	SPI2
Hardware CRC calculation	Y	Y
Rx/Tx FIFO	Y	Y
NSS pulse mode	Y	Y
I ² S mode	Y	Y
TI mode	Y	Y

3.16 High-definition multimedia interface (HDMI) – consumer electronics control (CEC)

The device embeds a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol.

3.17 Clock recovery system (CRS)

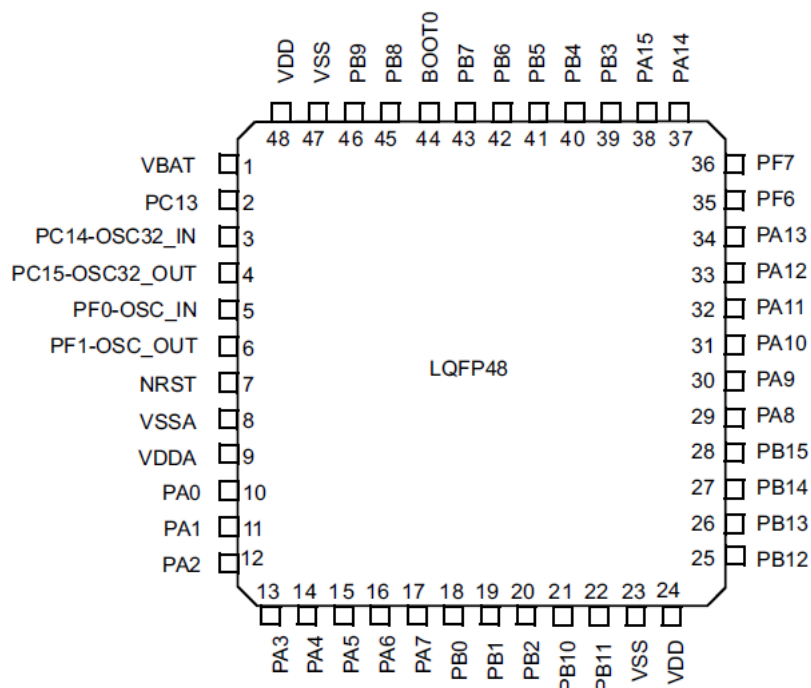
The FCM32x031x embeds a special block which allows automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range. This automatic trimming is based on the external synchronization signal, which could be either derived from USB SOF signalization, from LSE oscillator, from an external signal on CRS_SYNC pin or generated by user software.

3.18 Serial wire debug port (SWJ-DP)

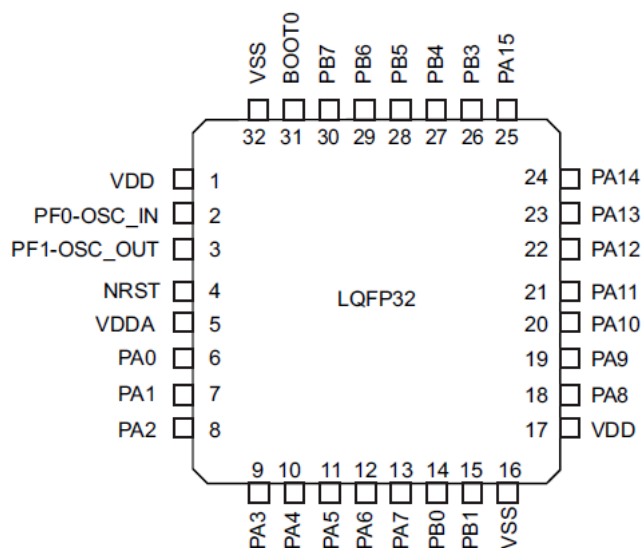
An ARM SWJ-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

4 Pinouts and pin descriptions

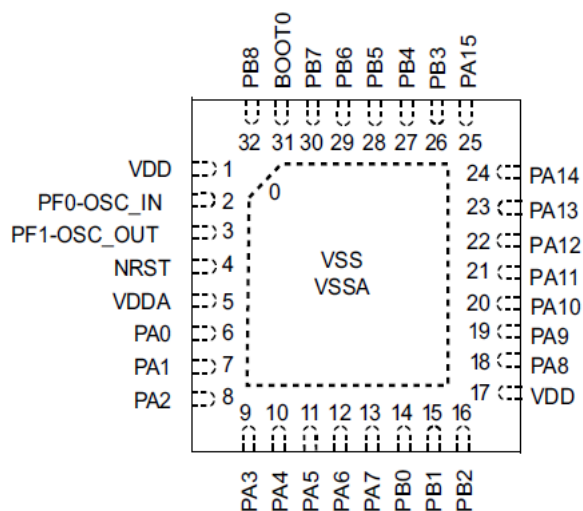
FCM32x031x LQFP48 pinout



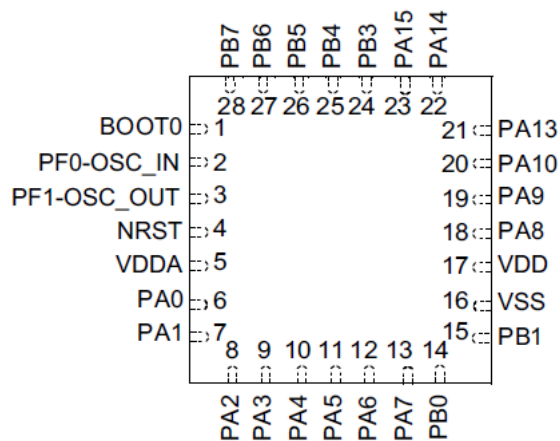
FCM32x031x LQFP32 pinout



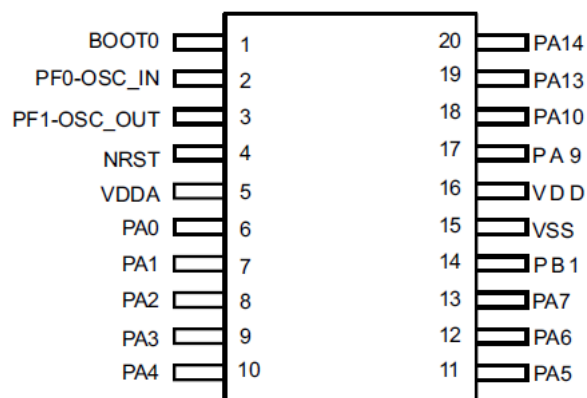
FCM32x031x UFQFPN32 pinout



FCM32x031xUFQFPN28 pinout



FCM32x031x TSSOP20 pinout



Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		FTf	5 V tolerant I/O, FM+ capable
		TTa	5 V tolerant I/O directly connected to ADC
		TC	Standard 5 V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

FCM32x031x Pin definitions

Pin number						Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48	LQFP32	UFQFPN32	UFQFPN28	WLCSP25	TSSOP20					Alternate functions	Additional functions
1	-	-	-	-	-	VBAT	S	-	-	Backup power supply	
2	-	-	-	-	-	PC13	I/O	TC	(1)(2)	-	RTC_TAMP1, RTC_TS, RTC_OUT, WKUP2
3	-	-	-	-	-	PC14-OSC32_IN (PC14)	I/O	TC	(1)(2)	-	OSC32_IN
4	-	-	-	-	-	PC15- OSC32_OUT (PC15)	I/O	TC	(1)(2)	-	OSC32_OUT

5	2	2	2	A5	2	PF0-OSC_IN (PF0)	I/O	FT	-	-	OSC_IN
6	3	3	3	B5	3	PF1-OSC_OUT (PF1)	I/O	FT	-	-	OSC_OUT
7	4	4	4	C5	4	NRST	I/O	RST	-	Device reset input / internal reset output (active low)	
8	-	0	-	E1	-	VSSA	S		-	Analog ground	
9	5	5	5	D5	5	VDDA	S		-	Analog power supply	
10	6	6	6	B4	6	PA0	I/O	TTa	-	TIM2_CH1_ETR, USART1_CTS	ADC_IN0, RTC_TAMP2, WKUP1
11	7	7	7	C4	7	PA1	I/O	TTa	-	TIM2_CH2, EVENTOUT, USART1_RTS	ADC_IN1
12	8	8	8	D4	8	PA2	I/O	TTa	-	TIM2_CH3, USART1_TX	ADC_IN2
13	9	9	9	E5	9	PA3	I/O	TTa	-	TIM2_CH4, USART1_RX	ADC_IN3
14	10	10	10	B3	10	PA4	I/O	TTa	-	SPI1_NSS, I2S1_WS, TIM14_CH1, USART1_CK	ADC_IN4
15	11	11	11	C3	11	PA5	I/O	TTa	-	SPI1_SCK, I2S1_CK, TIM2_CH1_ETR	ADC_IN5
16	12	12	12	D3	12	PA6	I/O	TTa	-	SPI1_MISO, I2S1_MCK, TIM3_CH1, TIM1_BKIN, TIM16_CH1, EVENTOUT	ADC_IN6

17	13	13	13	E4	13	PA7	I/O	TTa	-	SPI1_MOSI, I2S1_SD, TIM3_CH2, TIM14_CH1, TIM1_CH1N, TIM17_CH1, EVENTOUT	ADC_IN7
18	14	14	14	E3	-	PB0	I/O	TTa	-	TIM3_CH3, TIM1_CH2N, EVENTOUT	ADC_IN8
19	15	15	15	E2	14	PB1	I/O	TTa	-	TIM3_CH4, TIM14_CH1, TIM1_CH3N	ADC_IN9
20	-	16	-	-	-	PB2	I/O	FT	(3)		
21	-	-	-	-	-	PB10	I/O	FTf	-	TIM2_CH3, I2C1_SCL	-
22	-	-	-	-	-	PB11	I/O	FTf	-	TIM2_CH4, EVENTOUT, I2C1_SDA	-
23	16	0	16	E1	15	VSS	S	-	-	Ground	
24	17	17	17	D1	16	VDD	S	-	-	Digital power supply	
25	-	-	-	-	-	PB12	I/O	FT	-	TIM1_BKIN, EVENTOUT, SPI1_NSS	-
26	-	-	-	-	-	PB13	I/O	FT	-	TIM1_CH1N, SPI1_SCK	-
27	-	-	-	-	-	PB14	I/O	FT	-	TIM1_CH2N, SPI1_MISO	-
28	-	-	-	-	-	PB15	I/O	FT	-	TIM1_CH3N, SPI1_MOSI	RTC_REFIN
29	18	18	18	D2	-	PA8	I/O	FT	-	USART1_CK, TIM1_CH1, EVENTOUT, MCO	-

30	19	19	19	C1	17	PA9	I/O	FTf	-	USART1_TX, TIM1_CH2, I2C1_SCL	-
31	20	20	20	B1	18	PA10	I/O	FTf	-	USART1_RX, TIM1_CH3, TIM17_BKIN, I2C1_SDA	-
32	21	21	-	-	-	PA11	I/O	FT	-	USART1_CTS, TIM1_CH4, EVENTOUT	-
33	22	22	-	-	-	PA12	I/O	FT	-	USART1_RTS, TIM1_ETR, EVENTOUT	-
34	23	23	21	A1	19	PA13 (SWDIO)	I/O	FT	(4)	IR_OUT, SWDIO	-
35	-	-	-	-	-	PF6	I/O	FTf	-	I2C1_SCL	-
36	-	-	-	-	-	PF7	I/O	FTf	-	I2C1_SDA	-
37	24	24	22	A2	20	PA14 (SWCLK)	I/O	FT	(4)	USART1_TX, SWCLK	-
38	25	25	23	-	-	PA15	I/O	FT	-	SPI1_NSS, I2S1_WS, TIM2_CH_ETR, EVENTOUT, USART1_RX	-
39	26	26	24	-	-	PB3	I/O	FT	-	SPI1_SCK, I2S1_CK, TIM2_CH2, EVENTOUT	-
40	27	27	25	-	-	PB4	I/O	FT	-	SPI1_MISO, I2S1_MCK, TIM3_CH1, EVENTOUT	-

41	28	28	26	C2	-	PB5	I/O	FT	-	SPI1_MOSI, I2S1_SD, I2C1_SMBA, TIM16_BKIN, TIM3_CH2	-
42	29	29	27	B2	-	PB6	I/O	FTf	-	I2C1_SCL, USART1_TX, TIM16_CH1N	-
43	30	30	28	A3	-	PB7	I/O	FTf	-	I2C1_SDA, USART1_RX, TIM17_CH1N	-
44	31	31	1	A4	1	BOOT0	I	B	-	Boot memory selection	
45	-	32	-	-	-	PB8	I/O	FTf	(3)	I2C1_SCL, TIM16_CH1	-
46	-	-	-	-	-	PB9	I/O	FTf	-	I2C1_SDA, IR_OUT, TIM17_CH1, EVENTOUT	-
47	32	0	-	E1	-	VSS	S	-	-	Ground	
48	1	1	-	-	-	VDD	S	-	-	Digital power supply	

- PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
 - The speed should not exceed 2 MHz with a maximum load of 30 pF
 - These GPIOs must not be used as current sources (e.g. to drive an LED).
- After the first RTC domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers which are not reset by the system reset. For details on how to manage these GPIOs, refer to the RTC domain and RTC register descriptions in the reference manual.
- On the LQFP32 package, PB2 and PB8 should be treated as unconnected pins (even when they are not available on the package, they are not forced to a defined level by hardware).
After reset, these pins are configured as SWDIO and SWCLK alternate functions, and the internal pull-up on the SWDIO pin and the internal pull-down on the SWCLK pin are activated.

Alternate functions selected through GPIOA_AFR registers for port A

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	-	USART1_CTS	TIM2_CH1_ETR	-	-	-	-	-
PA1	EVENTOUT	USART1_RTS	TIM2_CH2	-	-	-	-	-
PA2	-	USART1_TX	TIM2_CH3	-	-	-	-	-
PA3	-	USART1_RX	TIM2_CH4	-	-	-	-	-
PA4	SPI1_NSS,I2S1_WS	USART1_CK	-	-	TIM14_CH1	-	-	-
PA5	SPI1_SCK,I2S1_CK	CEC	TIM2_CH1_ETR	-	-	-	-	-
PA6	SPI1_MISO,I2S1_MCK	TIM3_CH1	TIM1_BKIN	-	-	TIM16_CH1	EVENTOUT	-
PA7	SPI1_MOSI,I2S1_SD	TIM3_CH2	TIM1_CH1N	-	TIM14_CH1	TIM17_CH1	EVENTOUT	-
PA8	MCO	USART1_CK	TIM1_CH1	EVENTOUT	-	-	-	-
PA9	-	USART1_TX	TIM1_CH2	-	I2C1_SCL	MCO	-	-
PA10	TIM17_BKIN	USART1_RX	TIM1_CH3	-	I2C1_SDA	-	-	-
PA11	EVENTOUT	USART1_CTS	TIM1_CH4	-	-	I2C1_SCL	-	-
PA12	EVENTOUT	USART1_RTS	TIM1_ETR	-	-	I2C1_SDA	-	-
PA13	SWDIO	IR_OUT	-	-	-	-	-	-
PA14	SWCLK	USART1_TX	-	-	-	-	-	-
PA15	SPI1_NSS,I2S1_WS	USART1_RX	TIM2_CH1_ETR	EVENTOUT	-	-	-	-

Alternate functions selected through GPIOA_AFR registers for port B

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	EVENTOUT	TIM3_CH3	TIM1_CH2N	-	-	-	-	-
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	-	-	-	-	-
PB2	-	-	-	-	-	-	-	-
PB3	SPI1_SCK,I2S1_CK	EVENTOUT	TIM2_CH2	-	-	-	-	-
PB4	SPI1_MISO,I2S1_MCK	TIM3_CH1	EVENTOUT	-	-	TIM17_BKIN	-	-
PB5	SPI1_MOSI,I2S1_SD	TIM3_CH2	TIM16_BKIN	I2C1_SMBA	-	-	-	-
PB6	USART1_TX	I2C1_SCL	TIM16_CH1N	-	-	-	-	-
PB7	USART1_RX	I2C1_SDA	TIM17_CH1N	-	-	-	-	-
PB8	CEC	I2C1_SCL	TIM16_CH1	-	-	-	-	-
PB9	IR_OUT	I2C1_SDA	TIM17_CH1	EVENTOUT	-	SPI2_NSS	-	-
PB10	CEC	I2C1_SCL	TIM2_CH3	-	-	SPI2_SCK	-	-
PB11	EVENTOUT	I2C1_SDA	TIM2_CH4	-	-	-	-	-
PB12	SPI2_NSS,I2S2_WS	EVENTOUT	TIM1_BKIN	-	-	-	-	-
PB13	SPI2_SCK,I2S2_CK	-	TIM1_CH1N	-	-	I2C1_SCL	-	-
PB14	SPI2_MISO,I2S2_MCK	-	TIM1_CH2N	-	-	I2C1_SDA	-	-
PB15	SPI2_MOSI,I2S2_SD	-	TIM1_CH3N	-	-	-	-	-

Alternate functions selected through GPIOA_AFR registers for port F

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PF0	-	I2C1_SDA	-	-	-	-	-	-
PF1	-	I2C1_SCL	-	-	-	-	-	-

5 Memory mapping

To the difference of FCM32x031x4/x6, the code memory spaces end at 0x08003FFF and 0x08007FFF, respectively.

FCM32x031x4/x6 peripheral register boundary addresses

Bus	Boundary address	Size	Peripheral
	0x4800 1800 – 0x5FFF FFFF	~384 MB	-
AHB2	0x4800 1400 – 0x4800 17FF	1KB	GPIOF
	0x4800 0C00 – 0x4800 13FF	2KB	-
	0x4800 0800 – 0x4800 0BFF	1KB	GPIOC
	0x4800 0400 – 0x4800 07FF	1KB	GPIOB
	0x4800 0000 – 0x4800 03FF	1KB	GPIOA
		0x4002 4400 – 0x47FF FFFF	~128MB
AHB1	0x4002 4000 – 0x4002 43FF	1KB	TSC
	0x4002 3400 – 0x4002 3FFF	3KB	-
	0x4002 3000 – 0x4002 33FF	1KB	CRC
	0x4002 2400 – 0x4002 2FFF	3KB	-
	0x4002 2000 – 0x4002 23FF	1KB	Flash memory interface
	0x4002 1400 – 0x4002 1FFF	3KB	-
	0x4002 1000 – 0x4002 13FF	1KB	RCC
	0x4002 0400 – 0x4002 0FFF	3KB	-
	0x4002 0000 – 0x4002 03FF	1KB	DMA
	0x4001 8000 – 0x4001 FFFF	32KB	-
APB	0x4001 5C00 – 0x4001 7FFF	9KB	-
	0x4001 5800 – 0x4001 5BFF	1KB	DBGMCU
	0x4001 4C00 – 0x4001 57FF	3KB	-
	0x4001 4800 – 0x4001 4BFF	1KB	TIM17
	0x4001 4400 – 0x4001 47FF	1KB	TIM16
	0x4001 4000 – 0x4001 43FF	1KB	TIM15
	0x4001 3C00 – 0x4001 3FFF	1KB	-
	0x4001 3800 – 0x4001 3BFF	1KB	USART1
	0x4001 3400 – 0x4001 37FF	1KB	-
	0x4001 3000 – 0x4001 33FF	1KB	SPI1/I2S1
	0x4001 2C00 – 0x4001 2FFF	1KB	TIM1
	0x4001 2800 – 0x4001 2BFF	1KB	-
	0x4001 2400 – 0x4001 27FF	1KB	ADC
	0x4001 0800 – 0x4001 23FF	7KB	-
	0x4001 0400 – 0x4001 07FF	1KB	EXTI
	0x4001 0000 – 0x4001 03FF	1KB	SYSCFG
	0x4000 8000 – 0x4000 FFFF	32KB	-
	0x4000 7C00 – 0x4000 7FFF	1KB	-

0x4000 7800 – 0x4000 7BFF	1KB	CEC
0x4000 7400 – 0x4000 77FF	1KB	-
0x4000 7000 – 0x4000 73FF	1KB	PWR
0x4000 6C00 – 0x4000 6FFF	1KB	CRS
0x4000 6800 – 0x4000 6BFF	1KB	-
0x4000 6400 – 0x4000 67FF	1KB	CAN
0x4000 6000 – 0x4000 63FF	1KB	USB RAM
0x4000 5C00 – 0x4000 5FFF	1KB	USB
0x4000 5800 – 0x4000 5BFF	1KB	I2C2
0x4000 5400 – 0x4000 57FF	1KB	I2C1
0x4000 4800 – 0x4000 53FF	3KB	-
0x4000 4400 – 0x4000 47FF	1KB	USART2
0x4000 3C00 – 0x4000 43FF	2KB	-
0x4000 3800 – 0x4000 3BFF	1KB	SPI2
0x4000 3400 – 0x4000 37FF	1KB	-
0x4000 3000 – 0x4000 33FF	1KB	IWDG
0x4000 2C00 – 0x4000 2FFF	1KB	WWDG
0x4000 2800 – 0x4000 2BFF	1KB	RTC
0x4000 2400 – 0x4000 27FF	1KB	-
0x4000 2000 – 0x4000 23FF	1KB	TIM14
0x4000 1800 – 0x4000 1FFF	2KB	-
0x4000 1400 – 0x4000 17FF	1KB	TIM7
0x4000 1000 – 0x4000 13FF	1KB	TIM6
0x4000 0800 – 0x4000 0FFF	2KB	-
0x4000 0400 – 0x4000 07FF	1KB	TIM3
0x4000 0000 – 0x4000 03FF	1KB	TIM2

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS} .

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A = 25^\circ\text{C}$ and $T_A = T_{A\text{max}}$ (given by the selected temperature range).

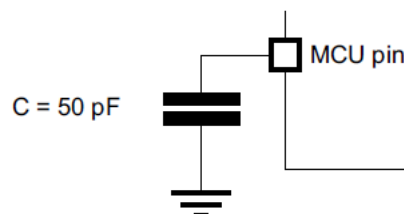
6.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A=25^\circ\text{C}$, $V_{DD}=V_{DDA}=3.3\text{V}$. They are given only as design guidelines and are not tested.

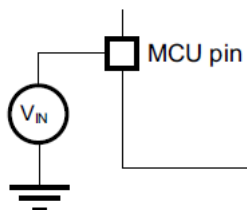
6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor



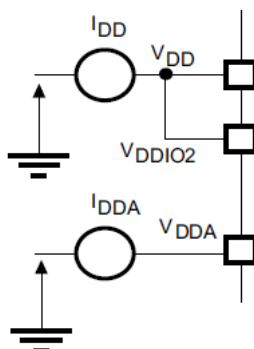
6.1.5 Pin input voltage



6.1.6 Power supply scheme

Each power supply pair (VDD/VSS, VDDA/VSSA etc.) must be decoupled with filtering ceramic capacitors. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

6.1.7 Current consumption measurement



6.2 Absolute maximum ratings

Exposure to maximum rating conditions for extended periods may affect device reliability.

Voltage characteristics

Symbol	Ratings	Min	Max	Unit
$V_{DD}-V_{SS}$	External main supply voltage	-0.3	5.8	V
$V_{DDIO2}-V_{SS}$	External I/O supply voltage	-0.3	5.8	V
$V_{DDA}-V_{SS}$	External analog supply voltage	-0.3	5.8	V
$V_{DD}-V_{DDA}$	Allowed voltage difference for $V_{DD}>V_{DDA}$	-	0.3	V
$V_{BAT}-V_{SS}$	External backup supply voltage	-0.3	5.8	V
V_{IN}	Input voltage on FT and FTf pins	$V_{SS}-0.3$	$V_{DDIO2}+0.3$	V
	Input voltage on TTa pins	$V_{SS}-0.3$	5.8	V

	Input voltage on any other pins	$V_{SS}-0.3$	5.8	V
$ \Delta V_{DDx} $	Variations between different V_{DD} power pins	-	50	mV
$ V_{SSx}-V_{SS} $	Variations between all the different ground pins	-	50	mV
$V_{ESD}(HBM)$	Electrostatic discharge voltage		3000	V

6.3 Operating conditions

6.3.1 General operating conditions

General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	48	MHz
f_{PCLK}	Internal APB clock frequency	-	0	48	MHz
V_{DD}	Standard operating voltage	-	1.8	5.5	V
V_{DDIO2}	I/O supply voltage		1.65	5.5	V
V_{DDA}	Analog operating voltage		V_{DD}	5.5	V
V_{BAT}	Backup operating voltage		2.1	5.5	V
V_{IN}	I/O input voltage	TC and RST I/O	-0.3	$V_{DDIOx}+0.3$	V
		TTa I/O	-0.3	$V_{DDA}+0.3$	
		FT and FTf I/O	-0.3	5.5	
P_D	Power dissipation at $T_A=85C$	LQFP48	-	350	mW
		UFQFPN48	-	600	
		LQFP32		350	
		UFQFPN32		500	
		UFQFPN28		170	
		TSSOP20		250	
TA	Ambient temperature for the suffix 6 version	Maximum power dissipation	-40	85	C
		Low power dissipation	-40	105	
	Ambient temperature for the suffix 7 version	Maximum power dissipation	-40	105	C
		Low power dissipation	-40	125	
TJ	Junction temperature range	Suffix 6 version	-40	105	C
		Suffix 7 version	-40	125	

6.3.2 Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	VDD rise time rate	-	0	∞	us/V
	VDD fall time rate		20	∞	

t _{VDDA}	VDDA rise time rate	-	0	∞	
	VDDA fall time rate		20	∞	

6.3.3 Embedded reset and power control block characteristics

Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{POR/PDR}	Power on/down reset threshold	Falling edge	1.51	1.58	1.65	V
		Rising edge	1.54	1.62	1.70	
V _{PDRhyst}	PDR hysteresis	-	-	40	-	mV
t _{RSTTEMPO}	Reset temporization	-	1.5	2.5	4.5	ms

Programmable voltage detector characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{PVD0}	PVD threshold 0	Falling edge	1.59	1.67	1.75	V
		Rising edge	1.75	1.83	1.91	
V _{PVD1}	PVD threshold 1	Falling edge	1.75	1.83	1.91	
		Rising edge	1.90	1.98	2.06	
V _{PVD2}	PVD threshold 2	Falling edge	1.90	1.98	2.06	
		Rising edge	2.06	2.14	2.22	
V _{PVD3}	PVD threshold 3	Falling edge	2.06	2.14	2.22	
		Rising edge	2.21	2.29	2.37	
V _{PVD4}	PVD threshold 4	Falling edge	2.21	2.29	2.37	
		Rising edge	2.35	2.43	2.51	
V _{PVD5}	PVD threshold 5	Falling edge	2.35	2.43	2.51	
		Rising edge	2.49	2.57	2.65	
V _{PVD6}	PVD threshold 6	Falling edge	2.49	2.57	2.65	
		Rising edge	2.64	2.72	2.80	
V _{PVD7}	PVD threshold 7	Falling edge	2.64	2.72	2.80	
		Rising edge	2.80	2.88	2.96	
V _{PVDhyst}	PVD hysteresis	-	-	160	-	mV
I _{DD(PVD)}	PVD current consumption	-	-	0.15	-	uA

6.3.4 Embedded reference voltage

Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{REFINT}	Internal reference voltage	-40C<TA<+105	1.22	1.23	1.24	V
t _{START}	ADC_IN17 buffer startup time	-	-	-	10	us
t _{s_vrefint}	ADC sampling time when	-	8	-	-	us

	reading the internal reference voltage					
$\Delta V_{REFINNT}$	Internal reference voltage spread over the temperature range	$V_{DDA}=3V$	-	-	10	mV
T_{Coeff}	Temperature coefficient	-	-100	-	100	ppm/C

6.3.5 Supply current characteristics

Typical current consumption (VDD+VDDA @ 3.6V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD}+I_{DDA}$	Run from Flash memory	All peripherals enabled, HSI 8MHz		3.7		mA
		All peripherals enabled, HSI48		15.0		
	Stop mode	Regulator in low-power mode, all oscillators OFF		6.2		uA
	Standby mode	Regulator in low-power mode, all oscillators OFF		6.0		uA

6.3.6 Wakeup time from low-power mode

Low-power mode wakeup timings

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{WUSTOP}	Wakeup from stop mode	Regulator in run mode	-	2.8	5	us
t_{START}		Regulator in low power mode		4.6	10	
$t_{WUSTANDBY}$	Wakeup from standby mode	-	-	50	-	
$t_{WUSLEEP}$	Wakeup from sleep mode	-	4 SYSCLK cycles			

6.3.7 External clock source characteristics

High-speed external user clock characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{HSE_EXT}	User external clock source frequency	-	8	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage	$0.7*V_{DDIOx}$	-	V_{DDIOx}	V
V_{HSEL}	OSC_IN input pin low level voltage	VSS	-	$0.3*V_{DDIOx}$	
$t_{W(HSEH)}$ $t_{W(HSEL)}$	OSC_IN high or low time	15	-	-	ns

$t_{r(HSE)}$	OSC_IN rise or fall time	-	-	20	
$t_{f(HSE)}$					

Low-speed external user clock characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSE_EXT}	User external clock source frequency	-	32.768	1000	KHz
V_{LSEH}	OSC32_IN input pin high level voltage	$0.7 \cdot V_{DDIOx}$	-	V_{DDIOx}	V
V_{LSEL}	OSC32_IN input pin low level voltage	VSS	-	$0.3 \cdot V_{DDIOx}$	
$t_{W(LSEH)}$	OSC32_IN high or low time	450	-	-	ns
$t_{W(LSEL)}$					
$t_{r(LSE)}$	OSC32_IN rise or fall time	-	-	50	
$t_{f(LSE)}$					

HSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	20	MHz
RF	Feedback resistor	-	-	200	-	K Ω
I_{DD}	HSE current consumption	$V_{DD}=3.3V$, $R_m=45 \Omega$, $CL=10pF@8MHz$		0.57		mA
g_m	Oscillator transconductance	Startup	10	-	-	mA/V
$t_{SU(HSE)}$	Startup time	VDD is stabilized	-	2	-	ms

LSE oscillator characteristics ($f_{LSE}=32.768KHz$)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	LSE current consumption	low drive capability		360		nA
		medium-low drive capability		450		
		medium-high drive capability		540		
		high drive capability		700		
g_m	Oscillator transconductance	low drive capability	5	-	-	uA/V
		medium-low drive capability	8			
		medium-high drive capability	15			
		high drive capability	25			
$t_{SU(LSE)}$	Startup time	V_{DDIOx} is stabilized	-	2	-	s

6.3.8 Internal clock source characteristics

HSI48 oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI48}	Frequency	-		48		MHz
TRIM	HSI48 user-trimming step	-		0.15		%
DuCy	Duty cycle	-	45	-	55	%
ACC _{HSI48}	Accuracy of the HSI48 oscillator(factory calibrated)	TA=-40 to 105 @SS	-1.84		2.00	%
		TA=-40 to 105@TT	-1.58		1.76	

		TA=-40 to 105@FF	-1.24		1.72	
t _{SU(HSI48)}	HSI48 oscillator startup time	-			6	us
I _{DDA(HSI48)}	HSI48 oscillator power consumption	-		643	801	uA

LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f _{LSI}	Frequency	-	31.9	40	55.5	KHz
t _{SU(LSI)}	LSI oscillator startup time	-			100	us
I _{DDA(LSI)}	LSI oscillator power consumption	-		400		nA

6.3.9 PLL characteristics

PLL characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f _{PLL_IN}	PLL input clock	1	8	24	MHz
t _{PLL_OUT}	PLL multiplier output clock	16		96	MHz
t _{LOCK}	PLL lock time	30		100	us
I _{DDA(PLL)}	PLL power consumption			350	uA
Jitter _{PLL}	Cycle-to-cycle jitter			300	ps

6.3.10 Memory characteristics

Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t _{PROG}	16-bit programming time	TA=-40 to +125			20	us
t _{ERASE}	Page(1KB) erase time				10	ms
t _{ME}	Mass erase time				40	ms
I _{DD}	Supply current	Write mode			3.5	mA
		Erase mode			2	mA
N _{END}	Endurance	TA=-40 to +125	20			kcycle
t _{RET}	Data retention	TA=25C	100			Year

6.3.11 EMC characteristics

EMC characteristics

Symbol	Parameter	Conditions	Level/Class
V _{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	VDD=3.3V, LQFP48, TA=25C, f _{HCLK} =48 MHz, conforming to IEC 61000-4-2	3B

V_{EFTB}	Fast transient voltage burst limits to be applied through 100pF on V_{DD} and V_{SS} pins to induce a functional disturbance	$V_{DD}=3.3V$, LQFP48, $T_A=25C$, $f_{HCLK}=48$ MHz, conforming to IEC 61000-4-4	4B
------------	--	--	----

EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. $[f_{HSE}/f_{HCLK}]$	Unit
				8/48 MHz	
SEMI	Peak level	$V_{DD}=3.6V$, $T_A=25C$, LQFP48 package compliant with IEC 61967-2	0.1 to 30MHz	-9	dBuV
			30 to 130MHz	9	
			130 MHz to 1GHz	17	
			EMI level	3	-

6.3.12 Electrical sensitivity characteristics

ESD absolute maximum ratings

Symbol	Parameter	Conditions	Packages	Class	Maxi value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	$T_A=+25C$, conforming to JESD22-A114	All	2	3000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	$T_A=+25C$, conforming to AEC-Q100-011	All	C6	1000	V

6.3.13 I/O current injection characteristics

I/O current injection susceptibility

Symbol	Parameter	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current	-5	+5	mA

6.3.14 I/O port characteristics

I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	TC and TTa I/O			$0.3 * V_{DDIOx}$	V
		FT and FTf I/O			$0.475 * V_{DDIOx} - 0.2$	
		All I/Os			$0.3 * V_{DDIOx}$	
V_{IH}	High level input voltage	TC and TTa I/O	$0.445 * V_{DDIOx} + 0.4$			V
		FT and FTf I/O	$0.5 * V_{DDIOx} + 0.2$			
		All I/Os	$0.7 * V_{DDIOx}$			

V_{hys}	Schmitt trigger hysteresis	TC and TTa I/O	200	mV
		FT and FTf I/O	100	
I_{lkg}	Input leakage current	TC, FT and FTf I/O TTa in digital mode $V_{SS} \leq V_{IN} \leq V_{DDIOx}$	± 0.1	μA
		TTa in digital mode $V_{DDIOx} \leq V_{IN} \leq V_{DDA}$	1	
		TTa in analog mode $V_{SS} \leq V_{IN} \leq V_{DDA}$	± 0.2	
		FT and FTf I/O $V_{DDIOx} \leq V_{IN} \leq 5V$	10	
R_{PU}	Weak pull-up resistor	$V_{IN} = V_{SS}$	40	$K \Omega$
R_{PD}	Weak pull-down resistor	$V_{IN} = -V_{DDIOx}$	40	$K \Omega$
C_{IO}	I/O pin capacitance		5	pF

Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage for an I/O pin	CMOS port $ I_{IO} = 8mA$ $V_{DDIOx} \geq 2.7V$	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		$V_{DDIOx} - 0.4$	-	
V_{OL}	Output low level voltage for an I/O pin	TTL port $ I_{IO} = 8mA$ $V_{DDIOx} \geq 2.7V$	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		2.4	-	
V_{OL}	Output low level voltage for an I/O pin	$ I_{IO} = 20mA$ $V_{DDIOx} \geq 2.7V$	-	1.3	V
V_{OH}	Output high level voltage for an I/O pin		$V_{DDIOx} - 1.3$	-	
V_{OL}	Output low level voltage for an I/O pin	$ I_{IO} = 6mA$ $V_{DDIOx} \geq 2.7V$	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		$V_{DDIOx} - 0.4$	-	
V_{OL}	Output low level voltage for an I/O pin	$ I_{IO} = 4mA$ $V_{DDIOx} \geq 2.7V$	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		$V_{DDIOx} - 0.4$	-	
V_{OLFM+}	Output low level voltage for an FTf I/O pin in FM+ mode	$ I_{IO} = 20mA$ $V_{DDIOx} \geq 2.7V$	-	0.4	V
			$ I_{IO} = 10mA$	-	

I/O AC characteristics

OSPEEDRy [1:0]	Symbol	Parameter	Conditions	Min	Max	Unit
x0	$f_{max(IO)out}$	Maximum frequency	$C_L = 50pF, V_{DDIOx} \geq 2V$	-	2	MHz
	$t_{f(IO)out}$	Output fall time		-	38	ns
	$t_{r(IO)out}$	Output rise time		-	39	
01	$f_{max(IO)out}$	Maximum frequency	$C_L = 50pF, V_{DDIOx} \geq 2V$	-	10	MHz

	$t_{f(I/O)out}$	Output fall time		-	25	ns
	$t_{r(I/O)out}$	Output rise time		-	25	
11	$f_{max(I/O)out}$	Maximum frequency	$C_L=30pF, V_{DDIOx} \geq 2.7V$	-	50	MHz
			$C_L=50pF, V_{DDIOx} \geq 2.7V$	-	30	
			$C_L=50pF, 2V \leq V_{DDIOx} < 2.7V$	-	20	
	$t_{f(I/O)out}$	Output fall time	$C_L=30pF, V_{DDIOx} \geq 2.7V$	-	6.5	ns
			$C_L=50pF, V_{DDIOx} \geq 2.7V$	-	9	
			$C_L=50pF, 2V \leq V_{DDIOx} < 2.7V$	-	15.5	
	$t_{r(I/O)out}$	Output rise time	$C_L=30pF, V_{DDIOx} \geq 2.7V$	-	6.6	
			$C_L=50pF, V_{DDIOx} \geq 2.7V$	-	8.6	
			$C_L=50pF, 2V \leq V_{DDIOx} < 2.7V$	-	39	
Fm+ configuratio n	$f_{max(I/O)out}$	Maximum frequency	$C_L=50pF, V_{DDIOx} \geq 2V$	-	2	MHz
	$t_{f(I/O)out}$	Output fall time		-	15.5	ns
	$t_{r(I/O)out}$	Output rise time		-	39	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	-	ns

6.3.15 NRST pin characteristics

NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	$0.3 \cdot V_{DD}$	V
$V_{IH(NRST)}$	NRST input high level voltage	-	$0.445 \cdot V_{DD} + 0.4$	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up resistor	$V_{IN} = V_{SS}$	-	40	-	K Ω
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	$2.7 < V_{DD} < 3.6$	300	-	-	ns
		$2.0 < V_{DD} < 3.6$	500	-	-	

6.3.16 ADC characteristics

ADC characteristics

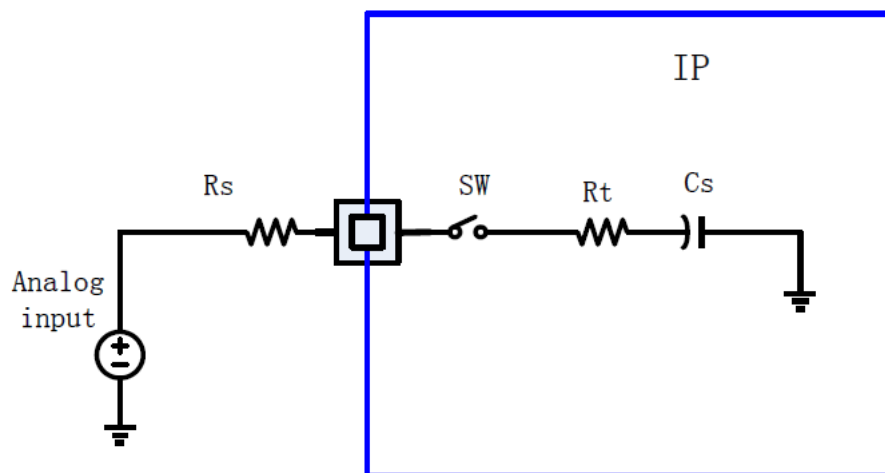
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.8	3.3	5.5	V
$I_{DD(ADC)}$	Current consumption of the ADC	$V_{DDA} = 3.3V$	-	1.1	-	mA
f_{ADC}	ADC clock frequency	-	-	-	16	MHz
f_S	Sampling rate	12-bit resolution	0.03	-	1	MHz
f_{TRIG}	External trigger frequency	12-bit resolution	-	-	18	$1/f_{ADC}$

V _{AIN}	Conversion voltage range		0		V _{DDA}	V
R _t	Input resistor during sampling	V _{DDA} =3V		0.5		k Ω
C _s	Internal sample and hold capacitor			26	30	pF
t _s	Sampling time	f _{ADC} =16MHz	4	-	-	1/f _{ADC}
t _{STAB}	Stabilization time		32	-	-	1/f _{ADC}
t _{CONV}	Total conversion time	12-bit resolution		12		1/f _{ADC}

ADC accuracy

Symbol	Parameter	Conditions	Typ	Max	Unit
ET	Total unadjusted error	f _{PCLK} =48MHz, f _{ADC} =16MHz, RAIN<10k Ω V _{DDA} =3V to 3.6V TA=25C	± 1.5	-	LSB
EO	Offset error		± 1.5	± 3.0	
EG	Gain error		± 2	± 5	
ED	Differential linearity error		± 0.6	± 1.5	
EL	Integral linearity error		± 1.5	± 3.0	

Analog Input Equivalent Circuit



$$R_s = \frac{T_{\text{samp}}}{10 * C_s} - R_t$$

RAIN max for f_{ADC} = 16 MHz

T _s (cycles)	t _s (us)	RAIN max (kΩ)
4	0.35	0.33
7.5	0.47	1.1
13.5	0.84	2.3
28.5	1.78	5.4
41.5	2.59	8.1
55.5	3.47	11.1
71.5	4.47	14.4
239.5	14.97	49.4

6.3.17 Temperature sensor characteristics

TS characteristics

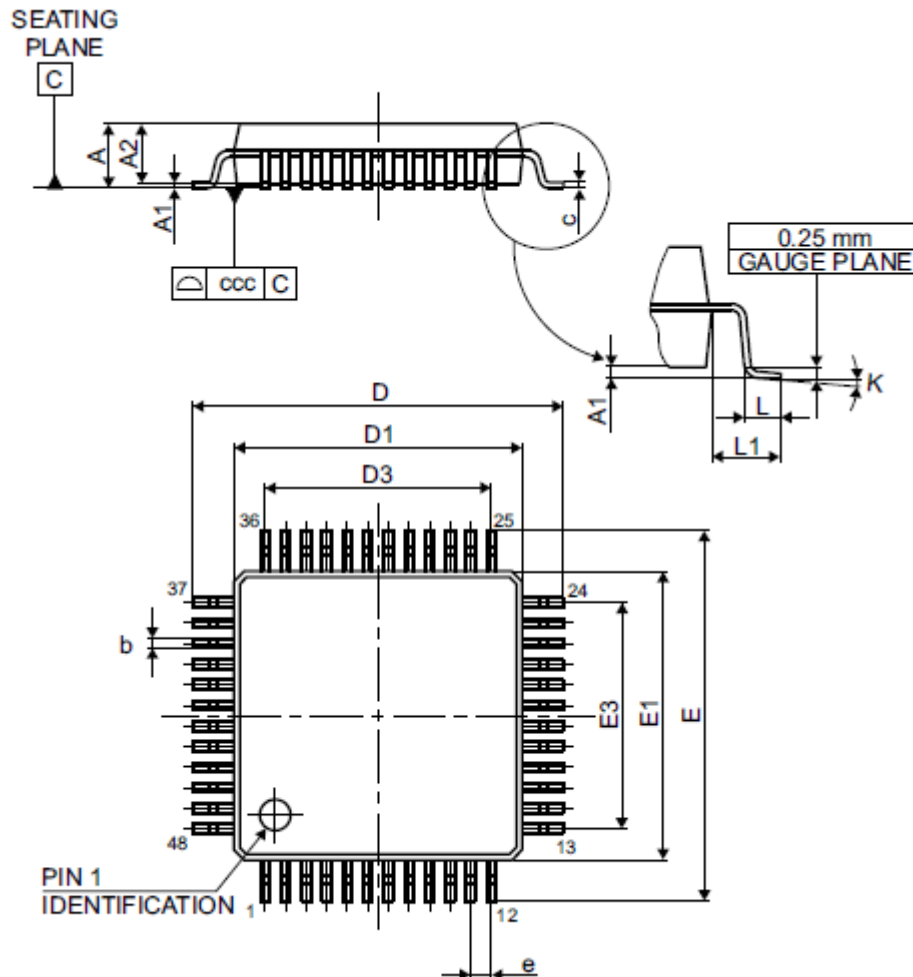
Symbol	Parameter	Min	Typ	Max	Unit
T _L	V _{SENSE} linearity with temperature	-	±1	±2	C
Avg_Slope	Average slope	4.2	4.28	4.36	mV/C
V30	Voltage at 30C	1.423	1.425	1.43	V
tSTART	ADC_IN16 buffer startup time	1	-	5	us
t _{s_temp}	ADC sampling time when reading the temperature	4	-	-	us

7 Package information

7.1 LQFP48 package information

LQFP48 is a 48-pin, 7 x 7 mm low-profile quad flat package.

LQFP48 package outline



LQFP48 package mechanical data

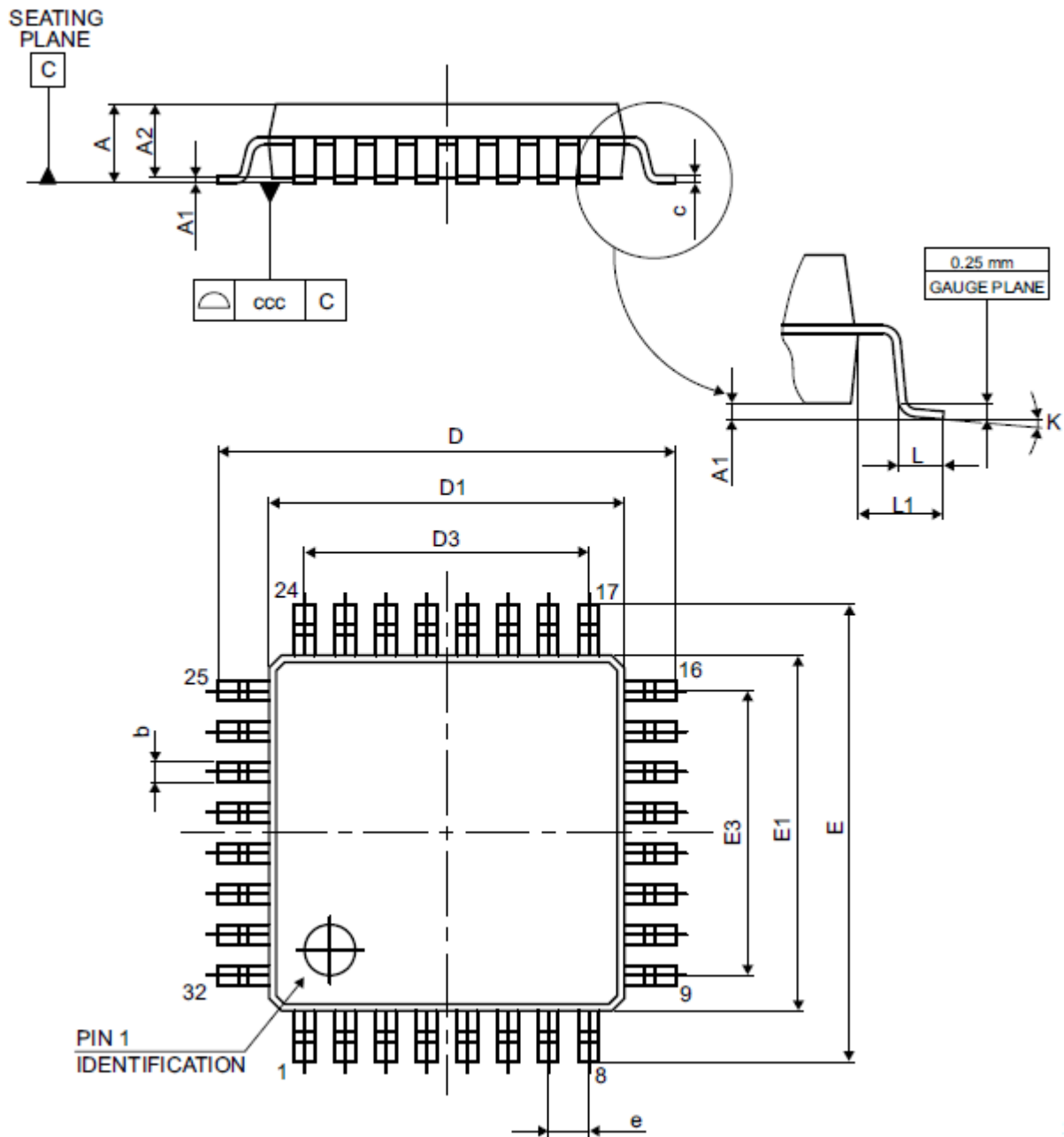
Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

7.2 LQFP32 package information

LQFP32 is a 32-pin, 7 x 7 mm low-profile quad flat package.

LQFP32 package outline



LQFP32 package mechanical data

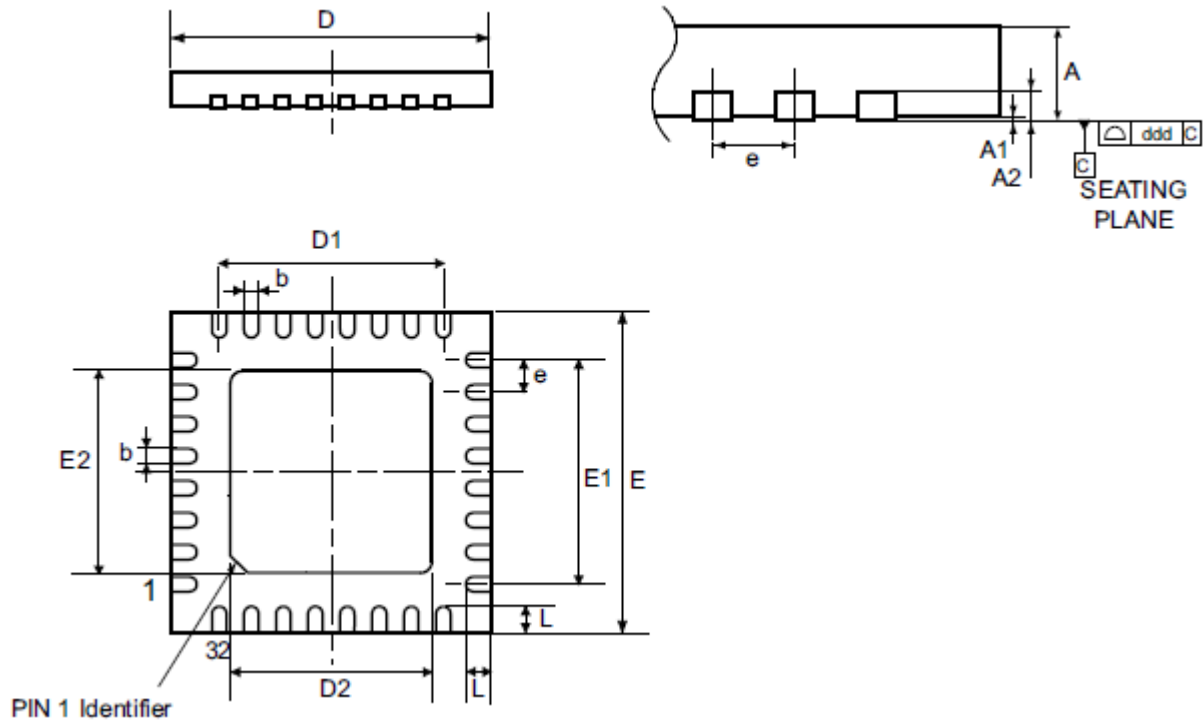
Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.600	-	-	0.2205	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.600	-	-	0.2205	-
e	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.

7.3 UFQFPN32 package information

UFQFPN32 is a 32-pin, 5 x 5 mm, 0.5 mm pitch fine-pitch quad flat package.

UFQFPN32 package outline



UFQFPN32 package mechanical data

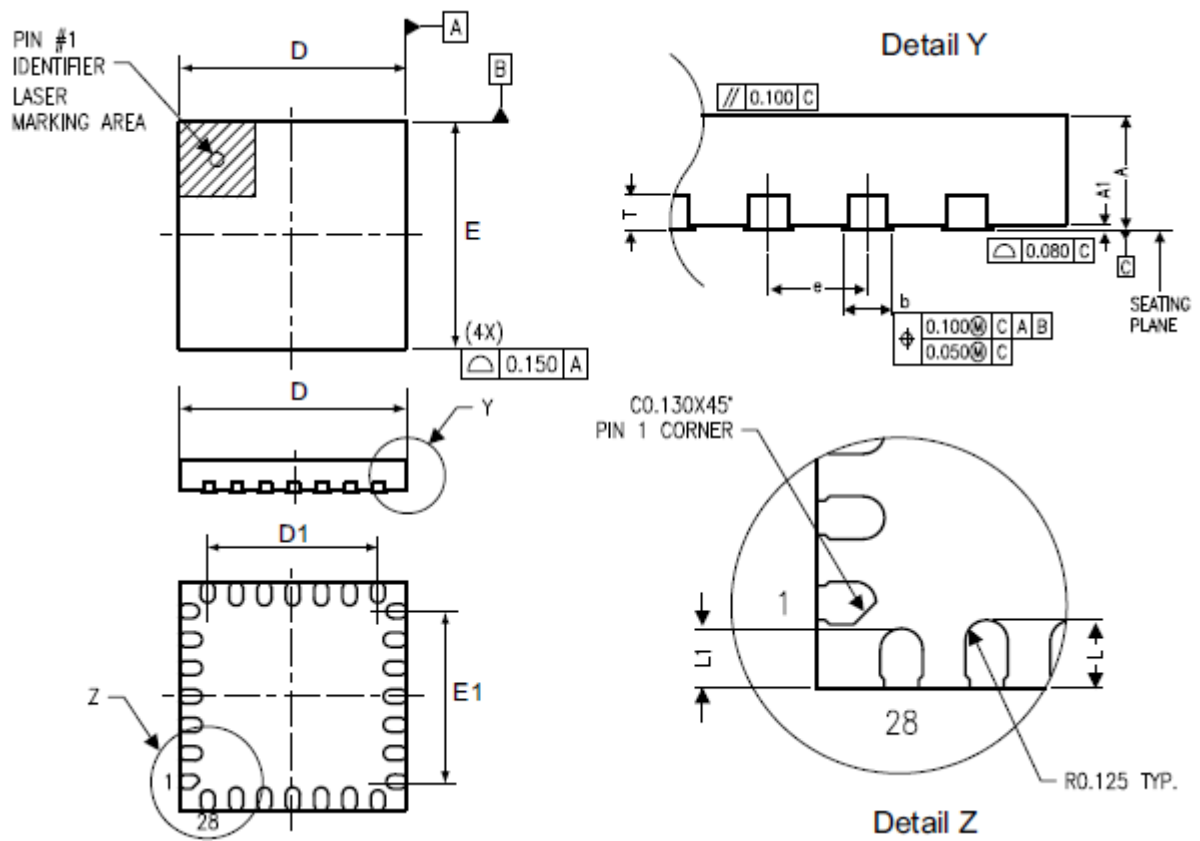
Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A		0.750			0.0296	
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.0060	-
b	0.180	0.230	0.280	0.0071	0.0091	0.0110
D	4.900	5.000	5.100	0.1929	0.1969	0.2008
D1	3.400	3.500	3.600	0.1339	0.1378	0.1417
D2	3.400	3.500	3.600	0.1339	0.1378	0.1417
E	4.900	5.000	5.100	0.1929	0.1969	0.2008
E1	3.400	3.500	3.600	0.1339	0.1378	0.1417
E2	3.400	3.500	3.600	0.1339	0.1378	0.1417
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

7.4 UFQFPN28 package information

UFQFPN28 is a 28-lead, 4 x 4 mm, 0.5 mm pitch, fine-pitch quad flat package.

UFQFPN28 package outline



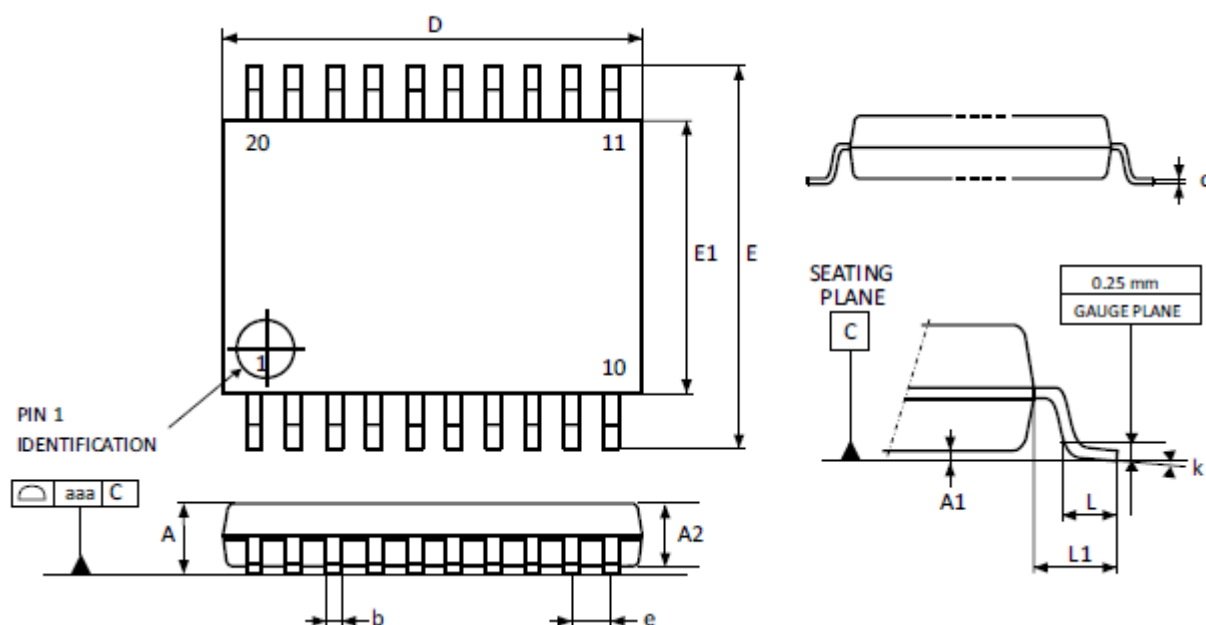
UFQFPN28 package mechanical data

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	-	0.000	0.050	-	0.0000	0.0020
D	3.900	4.000	4.100	0.1535	0.1575	0.1614
D1	2.900	3.000	3.100	0.1142	0.1181	0.1220
E	3.900	4.000	4.100	0.1535	0.1575	0.1614
E1	2.900	3.000	3.100	0.1142	0.1181	0.1220
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
L1	0.250	0.350	0.450	0.0098	0.0138	0.0177
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-

7.5 TSSOP20 package information

TSSOP20 is a 20-lead thin shrink small-outline, 6.5 x 4.4 mm, 0.65 mm pitch, package.

TSSOP20 package outline



TSSOP20 package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
c	0.090	-	0.200	0.0035	-	0.0079
D ⁽²⁾	6.400	6.500	6.600	0.2520	0.2559	0.2598
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1 ⁽³⁾	4.300	4.400	4.500	0.1693	0.1732	0.1772
e	-	0.650	-	-	0.0256	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	-	8°	0°	-	8°
aaa	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to four decimal digits.

8 Ordering information

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest FCM sales office.

Ordering information scheme

Example:	FCM32	F	031	C	6	T	6	- x
Device family FCM32 = FCM 32-bit microcontroller								
Product type F = General-purpose H = High performance								
Sub-family 031 = FCM32x031xx								
Pin count F = 20 pins G = 28 pins K = 32 pins T = 36 pins C = 48 pins								
User code memory size 4 = 16 Kbyte 6 = 32 Kbyte								
Package P = TSSOP T = LQFP U = UFQFPN Y = WLCSP								
Temperature range 6 = -40 to 85°C 7 = -40 to 105°C 8 = -40 to 125°C								
Options x = Revision code								

9 Revision history

Date	Revision	Changes
2020/1/17	0.1	Initial release
2020/3/11	0.2	3.5.1 Add VBAT description Add QFN pin assignment
2020/4/7	0.3	Table of CH 2: SPI/USART/I2C number change to 2; RAM change to 8KB; Add register map at CH 5; Add electrical characteristics at CH 6
2020/4/8	0.31	Fix error of 6.3.8 LSI $I_{DDA(LSI)}$ unit to nA
2020/5/21	0.32	Change SPI number to 2
2020/7/15	0.33	Add V_{REFINT} min/max value Change SPI number to 1 for device with pin number ≤ 32 Add index
2020/8/26	0.34	Add package information
2020/9/8	0.35	Add pin description and ordering information
2020/11/1	0.36	6.3.10 t_{ERASE} change from 5ms to 10ms
2020/11/26	0.37	6.3.16 Add RAIN max table

10 Others