

USBHD

USB Full speed Host/Device controller

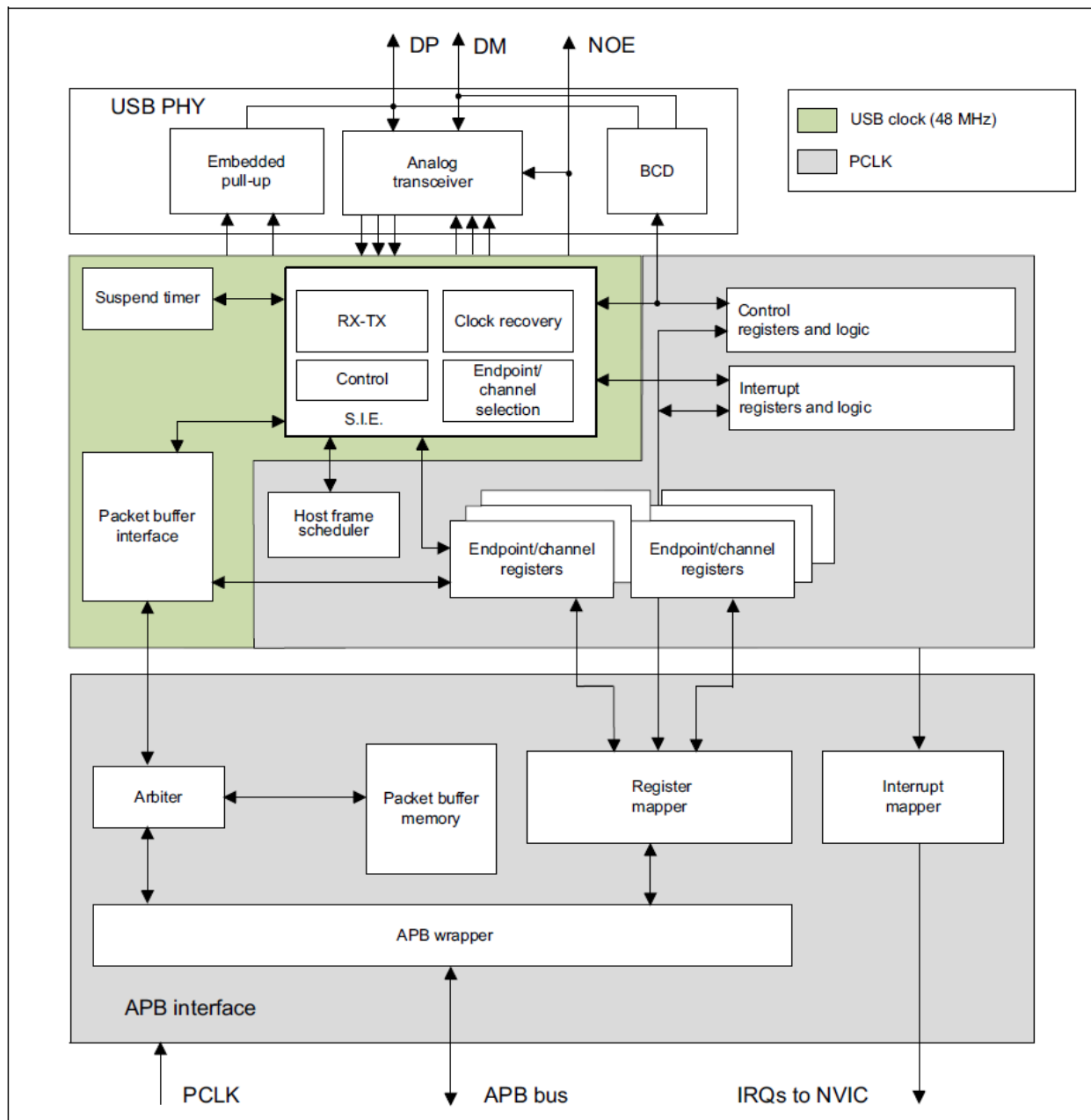
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1 简介

USBHD 为 USB 全速主/从 (HOST/DEVICE) 接口, 挂在 MCU 的 APB 总线上。

USBHD 支持休眠/唤醒, 可通过停止器件的时钟以降低电源消耗。



2 主要特征

- 兼容 USB 2.0 全速规范
- 支持主机/从机模式
- 可配置端口数从 1 至 8
- 专用的 2048 字节包缓冲存储 (SRAM)
- CRC 产生/检查; NRZI 编码/解码; 位填充
- 支持同步传输
- 支持双缓冲批量/同步端点
- USB 休眠/唤醒
- SOF 产生
- USB 2.0 LPM 支持 (仅从机模式)
- BCD 1.2 支持 (仅从机模式)
- USB 连接/断开控制 (集成 USB_DP 线上的上拉电阻)
- 主机支持全速/低速设备
- 主机支持连接 HUB
- 向下兼容 FCM32 系列的 USB device 接口, 可实现快速程序迁移

3 USBHD 实现

下表列出了该接口支持的功能。

| USB features | USB | | |
|---|---|----|----|
| | F0 | F1 | F3 |
| Host mode | X | X | X |
| Number of endpoints | 8 | 8 | 8 |
| Size of dedicated packet buffer memory SRAM | 1024 bytes ⁽¹⁾ 2048 bytes ⁽²⁾ | | |
| Dedicated packet buffer memory SRAM access scheme | 1x16 bits/word ⁽¹⁾ 2x16 bits/word ⁽²⁾ 1x32 bits/word ⁽²⁾ | | |
| USB 2.0 Link Power Management(LPM) support in device mode | X | X | X |
| Battery Charging Detection(BCD) support for device mode | X | X | X |
| Embedded pull-up resistor on USB_DP line | X | X | X |

x = 支持

(1) : USBHD_PMAS32B = 0

(2) : USBHD_PMAS32B = 1

4 USBHD 地址

USBHD 挂在 APB 总线上，其地址范围为 0x4000_5C00~0x4000_5FFF，大小为 1KB。

5 USBHD 控制位/寄存器

5.1 模块控制位

RCC_APB1ENR[23]: USBEN

RCC_APB1RSTR[23]: USBRST

USB_CFG (USB Configure Reg) – 0x4000_5C5C:

[15]: USBHD_EN, Host/Device Enable

0 = USBHD 兼容 F042/F072，没有 HOST 功能，复位后默认值

1 = USBHD 使能 HOST/DEVICE 功能，不兼容 F042/F072 的 DEVICE

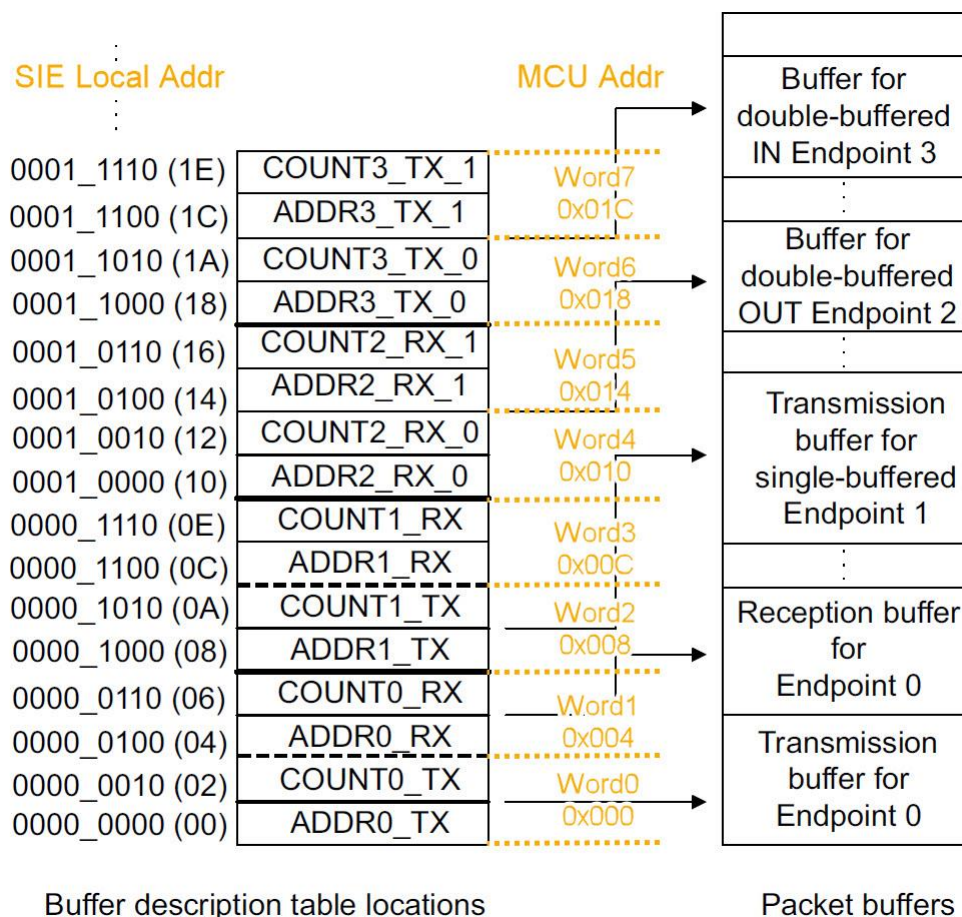
[14]: USBHD_PMAS32B, Packet Memory Access scheme 32-bits

0 = USB PM 按 16bits/word 访问，兼容 F1。F1 复位后默认值

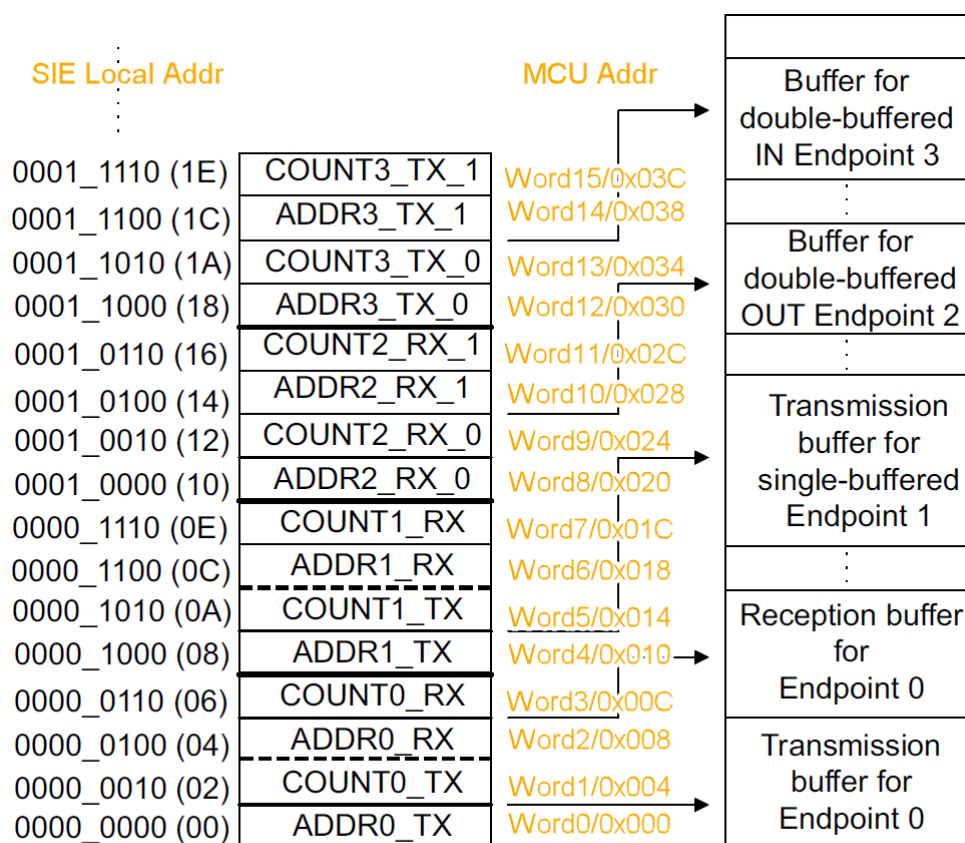
1 = USB PM 按 2x16bits/word 或 1x32bits/word 访问，兼容 F0/F3。F0/F3 复位后默认值

5.2 USBHD 通用寄存器

| Offset | Register | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | | |
|-----------|-------------|------|---------|-----------|------|------|--------|--------|-------|------|--------------|------|------|------|------|------|------|---------|---------------|---------|-------------|------------|----------|-----------|--------------|----------|--------|------|-------|-------|----------|---------|------|--------|--|--|--|
| 0x00 | USB_CHEP0R | Res. | Res. | Res. | Res. | Res. | ERR_RX | ERR_TX | LS_EP | NAK | DEVADDR[6:0] | | | | | | VTRX | DTOGRX | STAT_RX [1:0] | SETUP | UTYPE [1:0] | EPKIND | VTTX | DTOGTX | STAT_X [1:0] | EA[3:0] | | | | | | | | | | | |
| | Reset value | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| 0x04 | USB_CHEP1R | Res. | Res. | Res. | Res. | Res. | ERR_RX | ERR_TX | LS_EP | NAK | DEVADDR[6:0] | | | | | | VTRX | DTOGRX | STAT_RX [1:0] | SETUP | UTYPE [1:0] | EPKIND | VTTX | DTOGTX | STAT_X [1:0] | EA[3:0] | | | | | | | | | | | |
| | Reset value | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| 0x08 | USB_CHEP2R | Res. | Res. | Res. | Res. | Res. | ERR_RX | ERR_TX | LS_EP | NAK | DEVADDR[6:0] | | | | | | VTRX | DTOGRX | STAT_RX [1:0] | SETUP | UTYPE [1:0] | EPKIND | VTTX | DTOGTX | STAT_X [1:0] | EA[3:0] | | | | | | | | | | | |
| | Reset value | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| 0x0C | USB_CHEP3R | Res. | Res. | Res. | Res. | Res. | ERR_RX | ERR_TX | LS_EP | NAK | DEVADDR[6:0] | | | | | | VTRX | DTOGRX | STAT_RX [1:0] | SETUP | UTYPE [1:0] | EPKIND | VTTX | DTOGTX | STAT_X [1:0] | EA[3:0] | | | | | | | | | | | |
| | Reset value | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| 0x10 | USB_CHEP4R | Res. | Res. | Res. | Res. | Res. | ERR_RX | ERR_TX | LS_EP | NAK | DEVADDR[6:0] | | | | | | VTRX | DTOGRX | STAT_RX [1:0] | SETUP | UTYPE [1:0] | EPKIND | VTTX | DTOGTX | STAT_X [1:0] | EA[3:0] | | | | | | | | | | | |
| | Reset value | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| 0x14 | USB_CHEP5R | Res. | Res. | Res. | Res. | Res. | ERR_RX | ERR_TX | LS_EP | NAK | DEVADDR[6:0] | | | | | | VTRX | DTOGRX | STAT_RX [1:0] | SETUP | UTYPE [1:0] | EPKIND | VTTX | DTOGTX | STAT_X [1:0] | EA[3:0] | | | | | | | | | | | |
| | Reset value | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| 0x18 | USB_CHEP6R | Res. | Res. | Res. | Res. | Res. | ERR_RX | ERR_TX | LS_EP | NAK | DEVADDR[6:0] | | | | | | VTRX | DTOGRX | STAT_RX [1:0] | SETUP | UTYPE [1:0] | EPKIND | VTTX | DTOGTX | STAT_X [1:0] | EA[3:0] | | | | | | | | | | | |
| | Reset value | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| 0x1C | USB_CHEP7R | Res. | Res. | Res. | Res. | Res. | ERR_RX | ERR_TX | LS_EP | NAK | DEVADDR[6:0] | | | | | | VTRX | DTOGRX | STAT_RX [1:0] | SETUP | UTYPE [1:0] | EPKIND | VTTX | DTOGTX | STAT_X [1:0] | EA[3:0] | | | | | | | | | | | |
| | Reset value | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| 0x20-0x3F | Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x40 | USB_CNTR | Res. | HOST | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | THR512M | CTRM | PMAOVRM | ERRM | WKUPM | SUSPM | RST_DCONM | SOFM | ESOFM | L1REQM | Res. | L1RES | L2RES | SUSPEN | SUSPRDY | PDWN | USBRST | | | |
| | Reset value | | 0 | | | | | | | | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | | | |
| 0x44 | USB_ISTR | Res. | LS_DCON | DCON_STAT | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | THR512 | CTR | PMAOVR | ERR | WKUP | SUSP | RST_DCON | SOF | ESOF | L1REQ | Res. | Res. | DIR | IDN[3:0] | | | | | | |
| | Reset value | | 0 | 0 | | | | | | | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | |
| 0x48 | USB_FNR | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | RXDP | RXDM | LCK | LSOF [1:0] | FN[10:0] | | | | | | | | | | | | | | |
| | Reset value | | | | | | | | | | | | | | | | | | 0 | 0 | 0 | 0 | x | x | x | x | x | x | x | x | x | x | x | | | | |
| 0x4C | USB_DADDR | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | EF | ADD[6:0] | | | | | | | | | | | |
| | Reset value | | | | | | | | | | | | | | | | | | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | |



对于 16bit/word 的访问机制，其 BDT 分配如下示例（在逻辑及物理实现上一致，BDT 为 16 位，高 16 位未使用）：



Buffer description table locations

Packet buffers

由于其 RAM 高半字未使用，因此，RAM 容量减半。

7 USBHD 中断

USBHUB 的中断向量如下。

F0xx:

| Position | Priority | Type of Priority | Acronym | Description | Address |
|----------|----------|------------------|---------|--|-------------|
| ... | ... | ... | ... | ... | ... |
| 31 | 38 | settable | USBHD | USBHD global interrupt(combined with EXTI line 18) | 0x0000_00BC |

F1xx/F3xx:

| Position | Priority | Type of Priority | Acronym | Description | Address |
|----------|----------|------------------|---------|-------------|---------|
| ... | ... | ... | ... | ... | ... |

| | | | | | |
|-----|-----|----------|-----------------|--------------------------------|-------------|
| 19 | 26 | settable | USB_HP/CAN1_TX | USB High Priority/CAN1 TX | 0x0000 008C |
| 20 | 27 | settable | USB_LP/CAN1_RX0 | USB Low Priority/CAN1_RX0 | 0x0000 0090 |
| ... | ... | ... | ... | ... | ... |
| 42 | 49 | settable | USB_Wakeup | USB Wakeup(EXTI line 18) | 0x0000 00E8 |
| ... | ... | ... | ... | ... | ... |
| 74 | 81 | settable | USB_HP_RMP | USB High priority remap | 0x0000 0168 |
| 75 | 82 | settable | USB_LP_RMP | USB Low priority remap | 0x0000 016C |
| 76 | 83 | settable | USB_Wakeup_RMP | USB wakeup(EXTI line 18) remap | 0x0000 0170 |

8 USBHD 时钟

USBHD 的时钟频率必须为 48MHz。

RCC_CFGR2[27:24]: USBPRE2

| USBPRE2[3:0] | USBSW | PLLCLK (MHz) | USB CLOCK |
|--------------|-------|--------------|------------|
| 0 | 0 | - | HSI48 |
| | 1 | 48 | PLLCLK |
| 1 | 1 | 48 | PLLCLK |
| 2 | 1 | 72 | PLLCLK/1.5 |
| 3 | 1 | 96 | PLLCLK/2 |
| 4 | 1 | 120 | PLLCLK/2.5 |
| 5 | 1 | 144 | PLLCLK/3 |
| 6 | 1 | 168 | PLLCLK/3.5 |
| 7 | 1 | 192 | PLLCLK/4 |

9 版本历史

| Date | Revision | Author | Changes |
|-----------|----------|----------|---------|
| 2021/4/30 | 0.10 | Dick Hou | 初版 |
| 2023/6/20 | 0.11 | | 仅调整排版 |

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