ARM®-based 32-bit MCU, up to 64KB Flash, 8 timers, ADC & comm. interfaces, 1.8-5.5V

Features

- ARM® 32-bit Cortex-M0 CPU，frequency up to 48 MHz
- Memories
  - ✧ 16/32/64KB of Flash memory
  - ✧ 4/8 KB SRAM
- CRC calculation unit
- Reset and power management
  - ✧ Digital and I/Os supply: V_{DD} = 1.8 - 5.5V
  - ✧ Analog supply: V_{DDA} = 1.8 - 5.5V
  - ✧ Power-on/Power down reset(POR/PDR)
  - ✧ Programmable voltage detector(PVD)
  - ✧ Low power modes: Sleep, Stop, Standby
- Clock management
  - ✧ 4 to 24 MHz crystal oscillator
  - ✧ 32 kHz oscillator for RTC with calibration
  - ✧ Internal 8 MHz RC oscillator
  - ✧ Internal 40 kHz RC oscillator
  - ✧ PLL use for CPU clock
- Up to 39 fast I/Os
  - ✧ All mappable on external interrupt vectors
  - ✧ With 5V tolerant capability when power supply is 3V
- DMA controller
  - ✧ 5 channel
  - ✧ Support peripherals: TIMER/ADC/SPI/I^2C/USART
- One 12-bit, 1.0 us ADC(up to 10 channels)
  - ✧ Conversion range: 0 to 5.5 V
  - ✧ Embedded temp sensor
- 10 timers
  - ✧ One 16-bit advanced-control timer for timer for six channel PWM output
  - ✧ Six 16-bit timers, with up to four IC/OC,OCN, usable for IR control decoding
  - ✧ Independent and system watchdog timers
  - ✧ SysTick timer
- Communication interfaces
  - ✧ Two I^2C interfaces supporting Fast Mode Plus(1Mbit/s) with 20mA current sink, SMBus/PMBus and wakeup
  - ✧ Two USARTs supporting master synchronous SPI and modem control, one with ISO7816 interface LIN, IrDA, auto baud rate detection and wakeup feature
  - ✧ Two SPIs(50 Mbit/s) with 4 to 16 programmable bit frames, one with I^2S interface multiplexed
- HDMI CEC, wakeup on header reception
- Debug mode
  - ✧ Serial wire debug(SWD)
- 96-bit unique ID
- Packages
  - ✧ TSSOP20
  - ✧ LQFP32
  - ✧ LQFP48

Contents

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the FCM32x030x microcontrollers.

For information on the arm Cortex-M0 core, please refer to the Cortex-M0 Technical Reference Manual, available from the www.arm.com website.

2 Description

The FCM32x030x microcontrollers incorporate the high-performance arm Cortex-M0 32-bit RISC core operating at up to 48 MHz frequency, high-speed embedded memories (up to 64 Kbytes of Flash memory and 8 Kbytes of SRAM), and an extensive range of enhanced peripherals and I/Os. All devices offer standard communication interfaces (I^2C, SPI/I^2S, USART and HDMI-CEC), 12-bit ADC, five 16-bit General-purpose timers, one 16-bit advanced-control PWM timer.

The FCM32x030x microcontrollers operate in the -40 to +85C and -40 to +105C temperature ranges, from a 1.8 to 5.5 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

The FCM32x030x microcontrollers include devices in several different packages ranging from 20 pins to 48 pins with a die form also available upon request. Depending on the device chosen, different sets of peripherals are included.

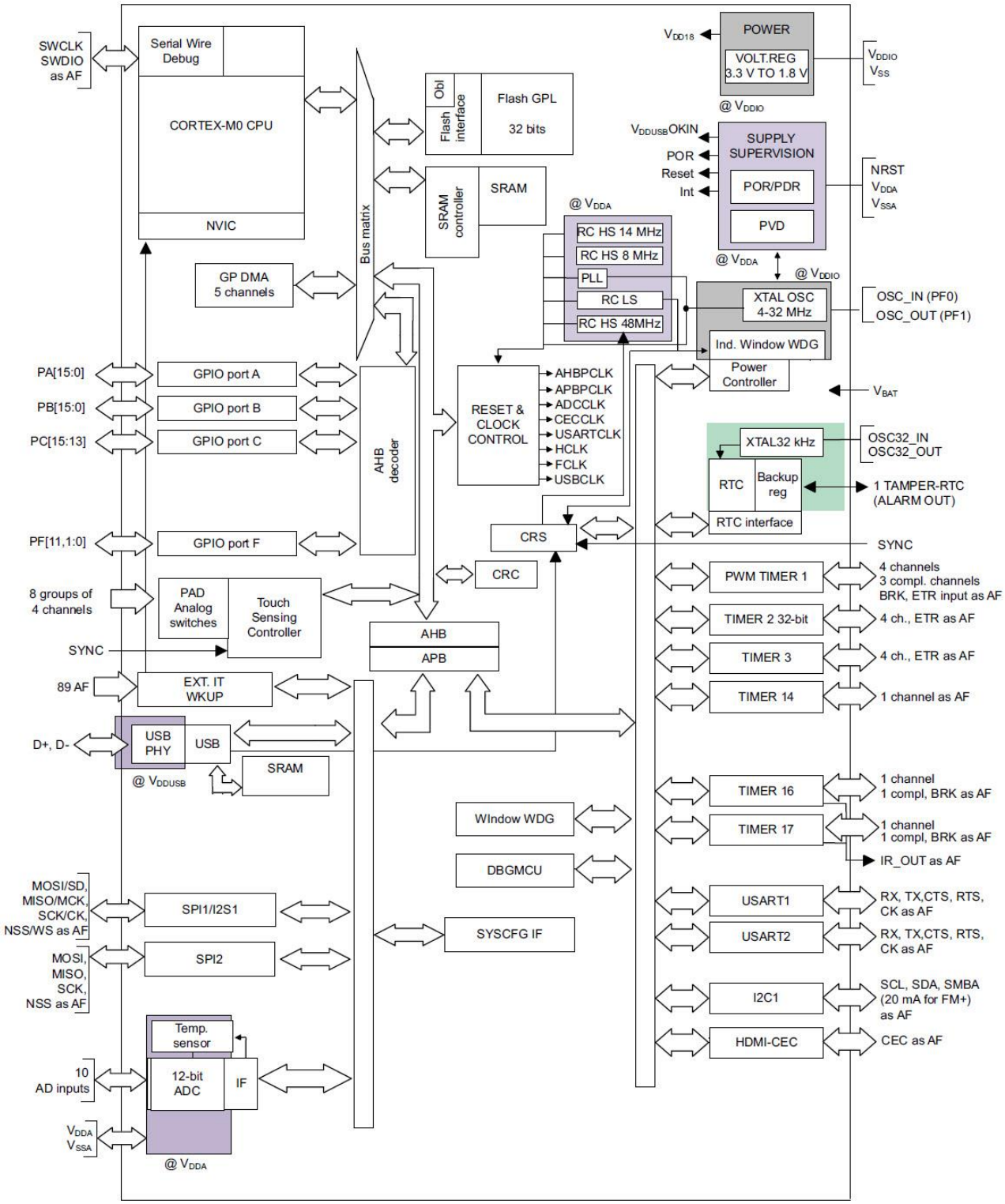
These features make the FCM32x030x microcontrollers suitable for a wide range of applications such as application control and user interfaces, hand-held equipment, A/V receivers and digital TV, PC peripherals, gaming and GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms and HVACs.

FCM32x030x medium-density device features and peripheral counts

Peripheral		FCM32F030F4	FCM32F030K6	FCM32F030C6	FCM32F030C8
Flash(Kbytes)		16	32	32	64
SRAM(Kbytes)		4			8
Timers	Advanced control	1 (16-bit)			
	General purpose	6 (16-bit)			
	Basic	-	-	-	1
Comm. interfaces	SPI/I2S(1)	1/1	1/1	2/2	2/2
	I2C	1			2
	USART	1			2
	CAN	0			
	CEC	0			
12-bit ADC (number of channels)		1 (11)	1 (12)		
GPIOs		15	26	39	
Max. CPU frequency		48 MHz			
Flash Turbo		-			
Operating voltage		1.8~5.5V			
Operating temperature		-40~85			
Packages		TSSOP20	LQFP32	LQFP48	

SPI1/2 interfaces can be used either in SPI mode or in I^2S audio mode.

Block diagram



3 Functional overview

3.1 ARM® Cortex-M0 core

ARM® Cortex-M0 is a generation of arm 32-bit RISC processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM® Cortex-M0 processors feature exceptional code-efficiency, delivering the high performance expected from an arm core, with memory sizes usually associated with 8- and 16-bit devices.

3.2 Memories

The device has he following features:

- 4/8 KB of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states
- The non-volatile memory is divided into two arrays:
  - 16/32/64 KB of embedded Flash memory for programs and data
  - Option Bytes

The option bytes are used to write-protect the memory (with 4 KB granularity) and/or readout-protect the whole memory with the following options:

- Level 0: no readout protection
- Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
- Level 2: chip readout protection, debug features(SWD) and boot in RAM selection disabled

3.3 Boot modes

At startup, the boot pin and boot selector option bits are used to select one of the three boot options:

- Boot from User Flash memory
- Boot from System Memory
- Boot from embedded SRAM

The boot pin is shared with the standard GPIO and can be disabled through the boot selector option bits. The boot loader is located in System Memory.

3.4 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a CRC-32 (Ethernet) polynomial.

3.5 Power management

3.5.1 Power supply

- V_{DD} = 1.8 - 5.5V: external power supply for I/Os and the internal regulator. It is provided externally through VDD pins.
- V_{DDA} = 1.8 - 5.5V: external analog power supply for ADC, Reset blocks, RC oscillator and PLL. The VDDA voltage level must be always greater or equal to the VDD voltage level and must be established first.

3.5.2 Power supply supervisors

The device has integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 1.8 V. The device remains in reset mode when the monitored supply voltage is below a specified threshold ($V_{POR/PDR}$) without the need for an external reset circuit.

- The POR monitors only the VDD supply voltage. During the startup phase it is required that VDDA should arrive first and be greater than or equal to VDD.
- The PDR monitors both the VDD and VDDA supply voltages, however the VDDA power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that VDDA is higher than or equal to VDD.

The device features an embedded programmable voltage detector (PVD) that monitors the VDD power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when VDD drops below the V_{PVD} threshold and/or when VDD is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.5.3 Voltage regulator

The regulator has two operating modes and it is always enabled after reset.

- Main (MR) is used in normal operating mode (RUN)
- Low power (LPR) can be used in Stop mode where the power demand is reduced.

In Standby mode, it is put in LPR mode. In this mode, MCU core and SRAM, SFRs and most peripherals stopped, the contents of the registers and SRAM are not lost.

3.5.4 Low-power modes

The FCM32x030x microcontrollers support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- Sleep mode
  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- Stop mode
  Stop mode achieves very low power consumption while retaining the content of SRAM and registers. All clocks in the 1.5 V domain are stopped, the PLL, the HIS RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or low power mode.
  The device can be woken up from Stop mode by any of the EXTI lines. The EXTI line source can be one of the 16 external lines, the PVD output, RTC, I^2C1, USART1, USB or the CEC.
  The CEC, USART1 and I^2C1 peripherals can be configured to enable the HIS RC oscillator so as to get clock for processing incoming data. If this is used when the voltage regulator is put in low power mode,

the regulator is first switched to normal mode before the clock is provided to the given peripheral.

- Standby mode
  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator enter LPR mode. PLL, the HIS RC and the HSE crystal oscillators are also switched off. The content of SRAM and registers are retained.
  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pins, or an RTC event occurs.

Note： The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

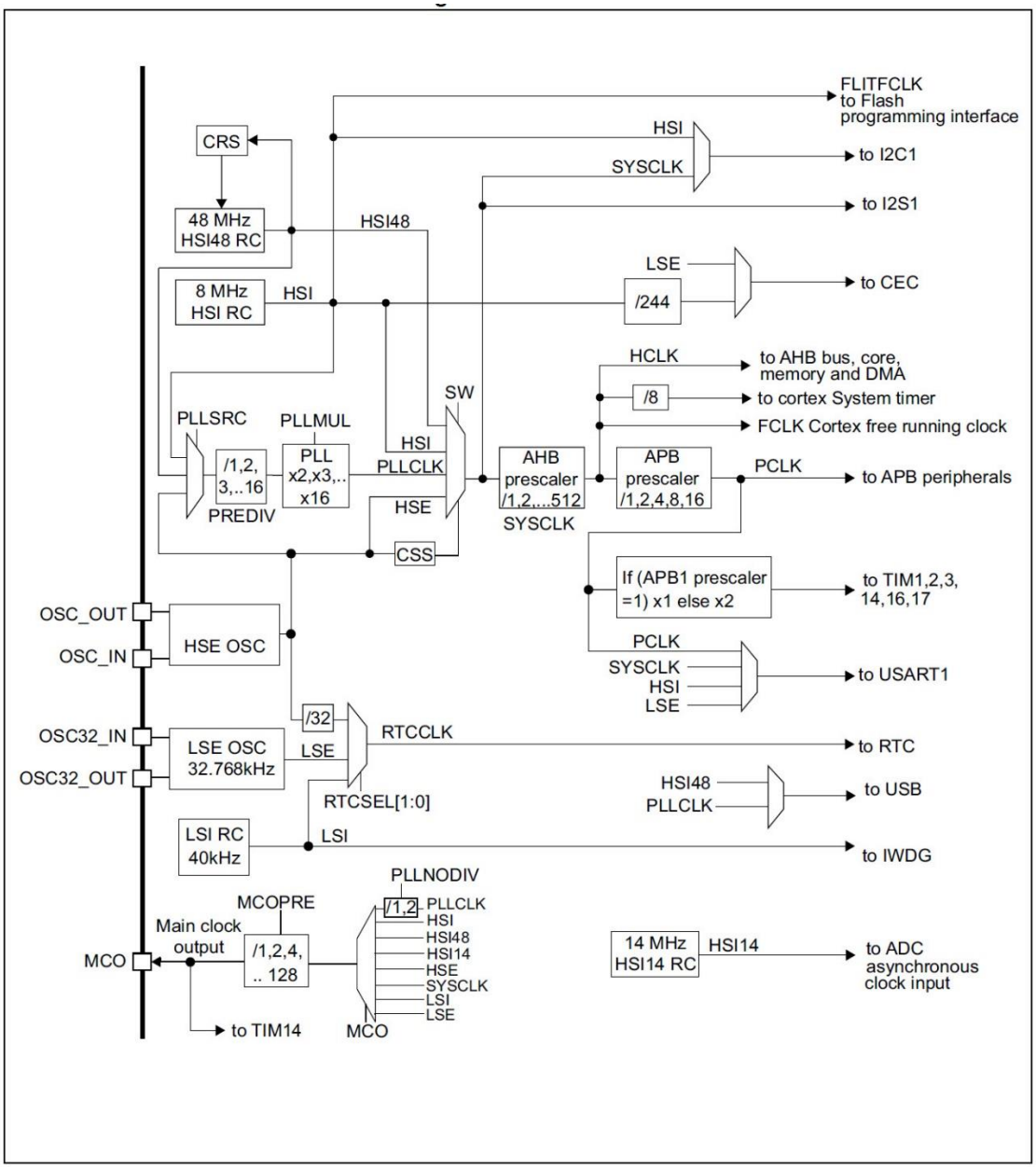
3.6 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary.

Several prescalers allow the application to configure the frequency of the AHB and the APB domains. The maximum frequency of the AHB and APB domains is 48 MHz.

Additionally, also the internal RC 48 MHz oscillator can be selected for system clock or PLL input source. This oscillator can be automatically fine-trimmed by the means of the CRS peripheral using the external synchronization.

Clock tree



3.7 GPIO

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

The I/O configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.8 Direct memory access controller (DMA)

The 5-channel general-purpose DMAs manage memory-to-memory, peripheral-to-memory and memory-to-

peripheral transfers.
The DMA supports circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.
Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.
DMA can be used with the main peripherals: SPIx, I2Sx, I2Cx, USARTx, all TIMx timers (except TIM14) and ADC.

3.9 Interrupts and events

3.9.1 Nested vectored interrupt controller (NVIC)

The FCM3F030x family embeds a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels (not including the 16 interrupt lines of Cortex-M0) and 4 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved

3.9.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 24 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect and external line with a pulse width shorter than the internal APB2 clock period. Up to 38 GPIOs can be connected to the 16 external lines.

3.10 Analog-to-digital converter (ADC)

The 12-bit analog-to-digital converter has up to 10 external and 3 internal (temperature sensor, voltage reference, VBAT voltage measurement) channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.
The ADC can be served by the DMA controller.
An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

3.10.1 Temperature sensor (TS)

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.
The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

3.10.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC. V_{REFINT} is internally connected to the ADC_IN17 input channel.

3.11 Timers and watchdogs

The FCM32x030x devices include up to 5 general-purpose timers and an advanced control timer.

Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	CCP channels	Complementary outputs
Advanced control	TIM1	16-bit	Up, down, Up/down	1~65536	Yes	4	Yes
General purpose	TIM2	16-bit	Up, down, Up/down	1~65536	Yes	4	No
	TIM3	16-bit	Up, down, Up/down	1~65536	Yes	4	No
	TIM14	16-bit	Up	1~65536	No	1	No
	TIM15	16-bit	Up	1~65536	Yes	2	No
	TIM16, TIM17	16-bit	Up	1~65536	Yes	1	Yes

3.11.1 Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on six channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers via the Timer Link feature for

synchronization of event chaining.

3.11.2 General-purpose timers (TIM2/3/14/15/16/17)

There are five general-purpose timers embedded in the FCM32x030x devices. Each general-purpose timer can be used to generate PWM outputs, or as simple time base.

TIM2/3

FCM32x030x devices feature two synchronizable 4-channel general-purpose timers. TIM2 is based on a 16-bit auto-reload up/down counter and a 16-bit prescaler. TIM3 is based on a 16-bit auto-reload up/down counter and a 16-bit prescaler. They feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.

The TIM2 and TIM3 general-purpose timers can work together or with the TIM1 advanced-control timer via the Timer Link feature for synchronization of event chaining.

TIM2 and TIM3 are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Their counters can be frozen in debug mode.

TIM14

This timer is based on a 16-bit auto-reload up counter and a 16-bit prescaler.

TIM14 features one single channel for input capture/output compare, PWM or one-pulse mode output.

Its counter can be frozen in debug mode.

TIM15/16/17

Both timers are based on a 16-bit auto-reload up counter and a 16-bit prescaler.

TIM15 has two independent channels, whereas TIM16 and TIM17 feature one single channel for input capture/output compare, PWM or one-pulse mode output.

The TIM15, TIM16 and TIM17 can work together.

They have a complementary output with dead-time generation and independent interrupt request generation.

Their counters can be frozen in debug mode.

3.11.3 Independent watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 12-bit down counter with user-defined refresh window. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.11.4 System window watchdog (WWDG)

The system window watchdog is based on a 7-bit down counter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PLCLK). It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.11.5 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter.

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source (HCLK or HCLK/8)

3.12 Real-time clock (RTC) and backup registers

The backup registers are five 32-bit registers used to store 20 bytes of user application data. They are not reset by a system or power reset, or at wake up from Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

- Calendar with subseconds, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- Automatic correction for 28, 29 (leap year), 30, and 31 day of the month
- Programmable alarm with wakeup from Stop and Standby mode capability
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize the RTC with a master clock
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy
- Two anti-tamper detection pins with programmable filter
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision

The RTC clock sources can be:

- A 32768 Hz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32

3.13 Inter-integrated circuit interface (I2C)

The I^2C interface can operate in multimaster or slave modes. It can support Standard mode (up to 100 kbit/s), Fast mode (up to 400 kbit/s) and Fast Mode Plus (up to 1Mbit/s) with 20mA output drive.

They supports 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (two addresses, one with configurable mask). It also includes programmable analog and digital noise filters.

In addition, I^2C1 provides hardware support for SMBUS 2.0 and PMBUS 1.1. It also has a clock domain independent from the CPU clock, allowing the I^2C1 to wake up the MCU from Stop mode on address match. The I^2C peripherals can be served by the DMA controller.

FCM32x030x I^2C implementation

I^2C features	I^2C1	I^2C2
7-bit addressing mode	Y	Y
10-bit addressing mode	Y	Y
Standard mode (up to 100 kbit/s)	Y	Y
Fast mode (up to 400 kbit/s)	Y	Y
Fast Mode Plus with 20mA output drive I/Os (up to 1Mbit/s)	Y	Y

Independent clock	Y	-
SMBus	Y	-
Wakeup from STOP	Y	-

3.14 Universal synchronous / asynchronous receiver / transmitter (USART)

The device embeds two universal synchronous/asynchronous receivers/transmitters (USART1, USART2) which communicate at speeds up to 12.5 Mbit/s.
They provide hardware management of the CTS, RTS and RS485 DE signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. USART1 supports also SmartCard communication (ISO7816), IrDA SIR ENDEC, LIN Master/Slave capability and auto baud rate feature, and has a clock domain independent to the CPU clock, allowing to wake up the MCU from Stop mode.
The USART interfaces can be served by the DMA controller.

FCM32x030x USART implementation

USART modes/ features	USART1	USART2
Hardware flow control for modem	Y	Y
Continuous communication using DMA	Y	Y
Multiprocessor communication	Y	Y
Synchronous mode	Y	Y
Smartcard mode	Y	-
Single-wire half-duplex communication	Y	Y
IrDA SIR ENDEC block	Y	-
LIN mode	Y	-
Dual clock domain and wakeup from Stop mode	Y	-
Receiver timeout interrupt	Y	-
Modbus communication	Y	-
Auto baud rate detection	Y	-
Driver Enable	Y	Y

3.15 Serial peripheral interface (SPI) / Inter-integrated sound interface (I^2S)

Two standard I^2S interface (multiplexed with SPI) supporting four different audio standards can operate as master or slave at half-duplex communication mode. It can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by an 8-bit programmable linear prescaler. When operating in master mode, it can output a clock for an external audio component at 256 times the sampling frequency.

FCM32x030x SPI/I^2S implementation

SPI features	SPI1	SPI2

Hardware CRC calculation	Y	Y
Rx/Tx FIFO	Y	Y
NSS pulse mode	Y	Y
I^2S mode	Y	Y
TI mode	Y	Y

3.16 High-definition multimedia interface (HDMI) – consumer electronics control (CEC)

The device embeds a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

3.17 Clock recovery system (CRS)

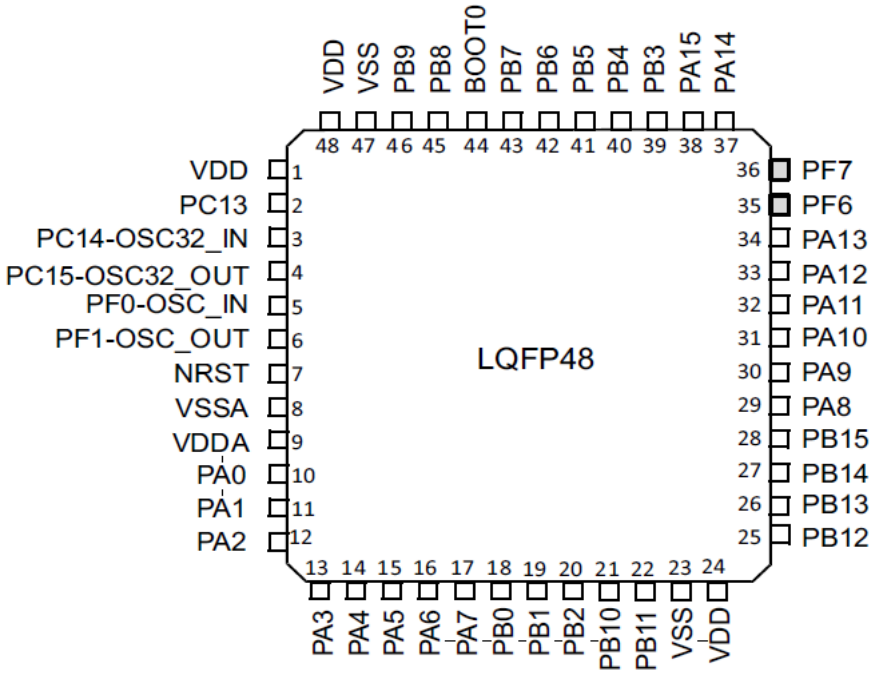
The FCM32x030x embeds a special block which allows automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range. This automatic trimming is based on the external synchronization signal, which could be either derived from LSE oscillator, from an external signal on CRS_SYNC pin or generated by user software.

3.18 Serial wire debug port (SWJ-DP)

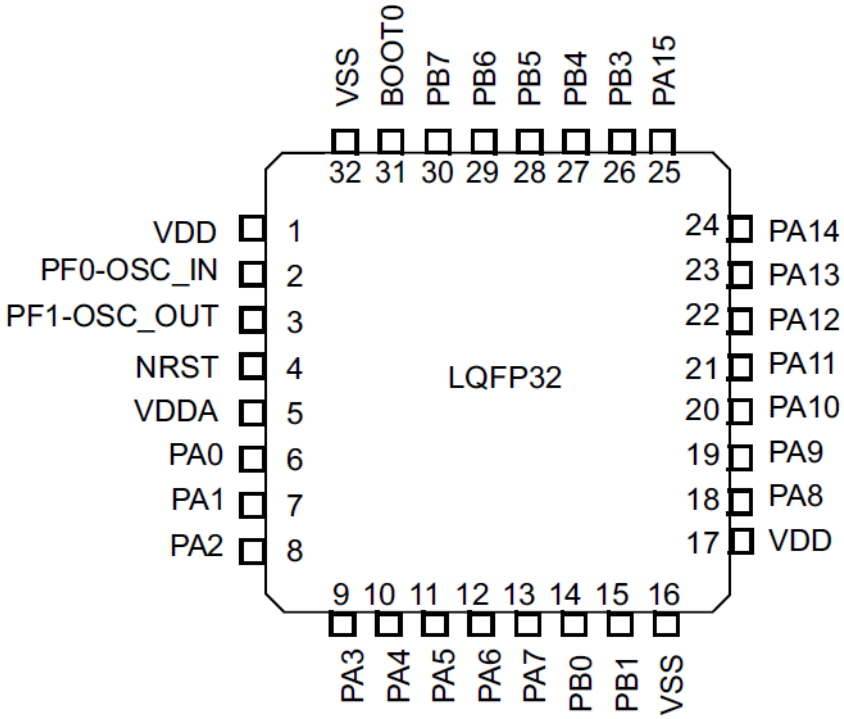
An ARM SWJ-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU, and support SWD.

4 Pinouts and pin descriptions

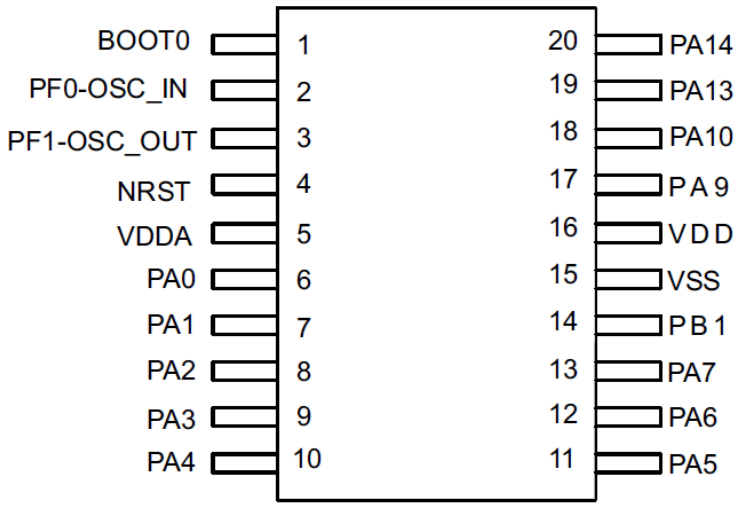
FCM32x030x LQFP48 pinout



FCM32x030x LQFP32 pinout



FCM32x030x TSSOP20 pinout



Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		FTf	5 V tolerant I/O, FM+ capable
		TTa	5 V tolerant I/O directly connected to ADC
		TC	Standard 5 V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

FCM32x030x pin definitions

Pin number			Pin name (function after reset)	Pin Type	I/O structure	Notes	Pin functions	
LQFP48	LQFP32	TSSOP20					Alternate functions	Additional functions
1	-	-	VDD	S			Complementary power supply	
2	-	-	PC13	I/O	TC	(1)	-	RTC_TAMP1, RTC_TS, RTC_OUT, WKUP2
3	-	-	PC14-OSC32_IN (PC14)	I/O	TC	(1)	-	OSC32_IN
4	-	-	PC15-OSC32_OUT (PC15)	I/O	TC	(1)	-	OSC32_OUT
5	2	2	PF0-OSC_IN (PF0)	I/O	FT		I2C1_SDA(5)	OSC_IN
6	3	3	PF1-OSC_OUT (PF1)	I/O	FT		I2C1_SCL(5)	OSC_OUT
7	4	4	NRST	I/O	RST		Device reset input / internal reset output (active low)	
8	-	-	VSSA	S			Analog ground	
9	5	5	VDDA	S			Analog power supply	
10	6	6	PA0	I/O	TTa		USART1_CTS(2), USART2_CTS(3)(5), USART4_TX(5)	ADC_IN0, RTC_TAMP2, WKUP1
11	7	7	PA1	I/O	TTa		USART1_RTS(2), USART2_RTS(3)(5), EVENTOUT, USART4_RX(5)	ADC_IN1
12	8	8	PA2	I/O	TTa		USART1_TX(2), USART2_TX(3)(5), TIM15_CH1(3)(5)	ADC_IN2
13	9	9	PA3	I/O	TTa		USART1_RX(2), USART2_RX(3)(5), TIM15_CH2(3)(5)	ADC_IN3
14	10	10	PA4	I/O	TTa		SPI1_NSS, USART1_CK(2) USART2_CK(3)(5), TIM14_CH1, USART6_TX(5)	ADC_IN4
15	11	11	PA5	I/O	TTa		SPI1_SCK, USART6_RX(5)	ADC_IN5
16	12	12	PA6	I/O	TTa		SPI1_MISO, TIM3_CH1, TIM1_BKIN, TIM16_CH1, EVENTOUT USART3_CTS(5)	ADC_IN6

17	13	13	PA7	I/O	TTa		SPI1_MOSI, TIM3_CH2, TIM14_CH1, TIM1_CH1N, TIM17_CH1, EVENTOUT	ADC_IN7
18	14	-	PB0	I/O	TTa		TIM3_CH3, TIM1_CH2N, EVENTOUT, USART3_CK(5)	ADC_IN8
19	15	14	PB1	I/O	TTa		TIM3_CH4, TIM14_CH1, TIM1_CH3N, USART3_RTS(5)	ADC_IN9
20	-	-	PB2	I/O	FT	(6)	-	-
21	-	-	PB10	I/O	FT		SPI2_SCK(5), I2C1_SCL(2), I2C2_SCL(3)(5), USART3_TX(5)	-
22	-	-	PB11	I/O	FT		I2C1_SDA(2), I2C2_SDA(3)(5), EVENTOUT, USART3_RX(5)	-
23	16	-	VSS	S			Ground	
24	17	16	VDD	S			Digital power supply	
25	-	-	PB12	I/O	FT		SPI1_NSS(2), SPI2_NSS(3)(5), TIM1_BKIN, EVENTOUT, USART3_CK(5)	-
26	-	-	PB13	I/O	FT		SPI1_SCK(2), SPI2_SCK(3)(5), I2C2_SDA, TIM1_CH1N, USART3_CTS(5)	-
27	-	-	PB14	I/O	FT		SPI1_MISO(2), SPI2_MISO(3)(5), I2C2_SDA(5), TIM1_CH2N, TIM15_CH1(3)(5), USART3_RTS(5)	-
28	-	-	PB15	I/O	FT		SPI1_MOSI(2), SPI2_MOSI(3)(5), TIM1_CH3N, TIM15_CH1N(3)(5), TIM15_CH2(3)(5)	RTC_REFIN
29	18	-	PA8	I/O	FT		USART1_CK, TIM1_CH1, EVENTOUT, MCO	-
30	19	17	PA9	I/O	FT		USART1_TX, TIM1_CH2, TIM15_BKIN(3)(5) I2C1_SCL(2)(5)	-

31	20	18	PA10	I/O	FT		USART1_RX, TIM1_CH3, TIM17_BKIN I2C1_SDA(2)(5)	-
32	21	-	PA11	I/O	FT		USART1_CTS, TIM1_CH4, EVENTOUT, I2C2_SCL(5)	-
33	22	-	PA12	I/O	FT		USART1_RTS, TIM1_ETR, EVENTOUT, I2C2_SDA(5)	-
34	23	19	PA13 (SWDIO)	I/O	FT	(7)	IR_OUT, SWDIO	-
35	-	-	PF6	I/O	FT	(4)	I2C1_SCL(2), I2C2_SCL(3)	-
36	-	-	PF7	I/O	FT	(4)	I2C1_SDA(2), I2C2_SDA(3)	-
37	24	20	PA14 (SWCLK)	I/O	FT	(7)	USART1_TX(2), USART2_TX(3)(5), SWCLK	-
38	25	-	PA15	I/O	FT		SPI1_NSS, USART1_RX(2), USART2_RX(3)(5), USART4_RTS(5), EVENTOUT	-
39	26	-	PB3	I/O	FT		SPI1_SCK, EVENTOUT, USART5_TX(5)	-
40	27	-	PB4	I/O	FT		SPI1_MISO, TIM3_CH1, EVENTOUT, TIM17_BKIN(5), USART5_RX(5)	-
41	28	-	PB5	I/O	FT		SPI1_MOSI, I2C1_SMBA, TIM16_BKIN, TIM3_CH2, USART5_CK_RTS(5)	-
42	29	-	PB6	I/O	FTf		I2C1_SCL, USART1_TX, TIM16_CH1N	-
43	30	-	PB7	I/O	FTf		I2C1_SDA, USART1_RX, TIM17_CH1N, USART4_CTS(5)	-
44	31	1	BOOT0	I	B		Boot memory selection	
45	-	-	PB8	I/O	FTf	(7)	I2C1_SCL, TIM16_CH1	-
46	-	-	PB9	I/O	FTf		I2C1_SDA, IR_OUT, SPI2_NSS(5), TIM17_CH1, EVENTOUT	-

47	32	15	VSS	S			Ground
48	1	16	VDD	S			Digital power supply

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF.
   - These GPIOs must not be used as current sources (e.g. to drive an LED).
2. On LQFP32 package, PB2 and PB8 should be treated as unconnected pins (even when they are not available on the package, they are not forced to a defined level by hardware).
3. After reset, these pins are configured as SWDIO and SWCLK alternate functions, and the internal pull-up on SWDIO pin and internal pull-down on SWCLK pin are activated.

Alternate functions selected through GPIOA_AFR registers for port A

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	-	USART2_CTS	TIM2_CH1_ETR	TSC_G1_IO1	-	-	-	-
PA1	EVENTOUT	USART2_RTS	TIM2_CH2	TSC_G1_IO2	-	-	-	-
PA2	-	USART2_TX	TIM2_CH3	TSC_G1_IO3	-	-	-	-
PA3	-	USART2_RX	TIM2_CH4	TSC_G1_IO4	-	-	-	-
PA4	SPI1_NSS,I2S1_WS	USART2_CK	USB_NOE	TSC_G2_IO1	TIM14_CH1	-	-	-
PA5	SPI1_SCK,I2S1_CK	CEC	TIM2_CH1_ETR	TSC_G2_IO2	-	-	-	-
PA6	SPI1_MISO,I2S1_MCK	TIM3_CH1	TIM1_BKIN	TSC_G2_IO3	-	TIM16_CH1	EVENTOUT	-
PA7	SPI1_MOSI,I2S1_SD	TIM3_CH2	TIM1_CH1N	TSC_G2_IO4	TIM14_CH1	TIM17_CH1	EVENTOUT	
PA8	MCO	USART1_CK	TIM1_CH1	EVENTOUT	CRS_SYNC	-	-	-
PA9	-	USART1_TX	TIM1_CH2	TSC_G4_IO1	I2C1_SCL	MCO	-	-
PA10	TIM17_BKIN	USART1_RX	TIM1_CH3	TSC_G4_IO2	I2C1_SDA	-	-	-
PA11	EVENTOUT	USART1_CTS	TIM1_CH4	TSC_G4_IO3	CAN_RX	I2C1_SCL	-	-
PA12	EVENTOUT	USART1_RTS	TIM1_ETR	TSC_G4_IO4	CAN_TX	I2C1_SDA	-	-
PA13	SWDIO	IR_OUT	USB_NOE	-	-	-	-	-
PA14	SWCLK	USART2_TX	-	-	-	-	-	-
PA15	SPI1_NSS,I2S1_WS	USART2_RX	TIM2_CH1_ETR	EVENTOUT	-	USB_NOE		

Alternate functions selected through GPIOA_AFR registers for port B

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	EVENTOUT	TIM3_CH3	TIM1_CH2N	TSC_G3_IO2	-	-	-	-
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	TSC_G3_IO3	-	-	-	-
PB2	-	-	-	TSC_G3_IO4	-	-	-	-
PB3	SPI1_SCK,I2S1_CK	EVENTOUT	TIM2_CH2	TSC_G5_IO1	-	-	-	-
PB4	SPI1_MISO,I2S1_MCK	TIM3_CH1	EVENTOUT	TSC_G5_IO2	-	TIM17_BKIN	-	-
PB5	SPI1_MOSI,I2S1_SD	TIM3_CH2	TIM16_BKIN	I2C1_SMBA	-	-	-	-
PB6	USART1_TX	I2C1_SCL	TIM16_CH1N	TSC_G5_IO3	-	-	-	-
PB7	USART1_RX	I2C1_SDA	TIM17_CH1N	TSC_G5_IO4	-	-	-	-
PB8	CEC	I2C1_SCL	TIM16_CH1	TSC_SYNC	CAN_RX	-	-	-
PB9	IR_OUT	I2C1_SDA	TIM17_CH1	EVENTOUT	CAN_TX	SPI2_NSS	-	-
PB10	CEC	I2C2_SCL(1)	TIM2_CH3	TSC_SYNC	-	SPI2_SCK	-	-
PB11	EVENTOUT	I2C2_SDA(1)	TIM2_CH4	-	-	-	-	-
PB12	SPI2_NSS,I2S2_WS	EVENTOUT	TIM1_BKIN	-	-	-	-	-
PB13	SPI2_SCK,I2S2_CK	-	TIM1_CH1N	-	-	I2C2_SCL(1)	-	-
PB14	SPI2_MISO,I2S2_MCK	-	TIM1_CH2N	-	-	I2C2_SDA(1)	-	-
PB15	SPI2_MOSI,I2S2_SD	-	TIM1_CH3N	-	-	-	-	-

(1) It is for I2C1 when only one I2C implement

Alternate functions selected through GPIOA_AFR registers for port F

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PF0	CRS_SYNC	I2C1_SDA	-	-	-	-	-	-
PF1	-	I2C1_SCL	-	-	-	-	-	-

5 Memory mapping

To the difference of FCM32x030x4/x6/x8, the code memory spaces end at 0x08003FFF, 0x08007FFF and 0x0800FFFF, respectively.

FCM32x030x4/x6/x8 peripheral register boundary addresses

Bus	Boundary address	Size	Peripheral
	0x4800 1800 – 0x5FFF FFFF	~384 MB	-
AHB2	0x4800 1400 – 0x4800 17FF	1KB	GPIOF
	0x4800 0C00 – 0x4800 13FF	2KB	-
	0x4800 0800 – 0x4800 0BFF	1KB	GPIOC
	0x4800 0400 – 0x4800 07FF	1KB	GPIOB
	0x4800 0000 – 0x4800 03FF	1KB	GPIOA
	0x4002 4400 – 0x47FF FFFF	~128MB	-
AHB1	0x4002 4000 – 0x4002 43FF	1KB	TSC
	0x4002 3400 – 0x4002 3FFF	3KB	-
	0x4002 3000 – 0x4002 33FF	1KB	CRC
	0x4002 2400 – 0x4002 2FFF	3KB	-
	0x4002 2000 – 0x4002 23FF	1KB	Flash memory interface
	0x4002 1400 – 0x4002 1FFF	3KB	-
	0x4002 1000 – 0x4002 13FF	1KB	RCC
	0x4002 0400 – 0x4002 0FFF	3KB	-
	0x4002 0000 – 0x4002 03FF	1KB	DMA
	0x4001 8000 – 0x4001 FFFF	32KB	-
APB	0x4001 5C00 – 0x4001 7FFF	9KB	-
	0x4001 5800 – 0x4001 5BFF	1KB	DBGMCU
	0x4001 4C00 – 0x4001 57FF	3KB	-
	0x4001 4800 – 0x4001 4BFF	1KB	TIM17
	0x4001 4400 – 0x4001 47FF	1KB	TIM16
	0x4001 4000 – 0x4001 43FF	1KB	TIM15
	0x4001 3C00 – 0x4001 3FFF	1KB	-
	0x4001 3800 – 0x4001 3BFF	1KB	USART1
	0x4001 3400 – 0x4001 37FF	1KB	-
	0x4001 3000 – 0x4001 33FF	1KB	SPI1/I2S1
	0x4001 2C00 – 0x4001 2FFF	1KB	TIM1
	0x4001 2800 – 0x4001 2BFF	1KB	-
	0x4001 2400 – 0x4001 27FF	1KB	ADC
	0x4001 0800 – 0x4001 23FF	7KB	-
	0x4001 0400 – 0x4001 07FF	1KB	EXTI
	0x4001 0000 – 0x4001 03FF	1KB	SYSCFG
	0x4000 8000 – 0x4000 FFFF	32KB	-

	0x4000 7C00 – 0x4000 7FFF	1KB	-
	0x4000 7800 – 0x4000 7BFF	1KB	CEC
	0x4000 7400 – 0x4000 77FF	1KB	-
	0x4000 7000 – 0x4000 73FF	1KB	PWR
	0x4000 6C00 – 0x4000 6FFF	1KB	CRS
	0x4000 6800 – 0x4000 6BFF	1KB	-
	0x4000 6400 – 0x4000 67FF	1KB	CAN
	0x4000 6000 – 0x4000 63FF	1KB	USB RAM
	0x4000 5C00 – 0x4000 5FFF	1KB	USB
	0x4000 5800 – 0x4000 5BFF	1KB	I2C2
	0x4000 5400 – 0x4000 57FF	1KB	I2C1
	0x4000 4800 – 0x4000 53FF	3KB	-
	0x4000 4400 – 0x4000 47FF	1KB	USART2
	0x4000 3C00 – 0x4000 43FF	2KB	-
	0x4000 3800 – 0x4000 3BFF	1KB	SPI2
	0x4000 3400 – 0x4000 37FF	1KB	-
	0x4000 3000 – 0x4000 33FF	1KB	IWDG
	0x4000 2C00 – 0x4000 2FFF	1KB	WWDG
	0x4000 2800 – 0x4000 2BFF	1KB	RTC
	0x4000 2400 – 0x4000 27FF	1KB	-
	0x4000 2000 – 0x4000 23FF	1KB	TIM14
	0x4000 1800 – 0x4000 1FFF	2KB	-
	0x4000 1400 – 0x4000 17FF	1KB	TIM7
	0x4000 1000 – 0x4000 13FF	1KB	TIM6
	0x4000 0800 – 0x4000 0FFF	2KB	-
	0x4000 0400 – 0x4000 07FF	1KB	TIM3
	0x4000 0000 – 0x4000 03FF	1KB	TIM2

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25C and T_A = $T_A$max (given by the selected temperature range).

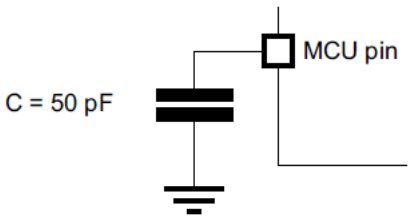
6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A=25C, VDD=VDDA=3.3V. They are given only as design guidelines and are not tested.

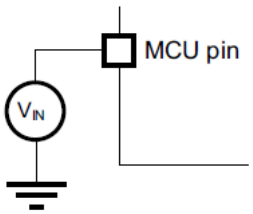
6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor



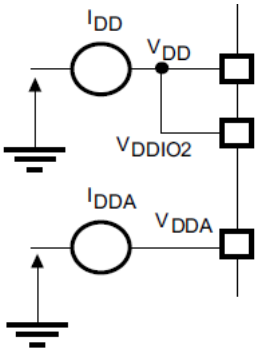
6.1.5 Pin input voltage



6.1.6 Power supply scheme

Each power supply pair (VDD/VSS, VDDA/VSSA etc.) must be decoupled with filtering ceramic capacitors. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

6.1.7 Current consumption measurement



6.2 Absolute maximum ratings

Exposure to maximum rating conditions for extended periods may affect device reliability.

Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}-V_{SS}	External main supply voltage	-0.3	5.8	V
V_{DDIO2}-V_{SS}	External I/O supply voltage	-0.3	5.8	V
V_{DDA}-V_{SS}	External analog supply voltage	-0.3	5.8	V

V_{DD}-V_{DDA}	Allowed voltage difference for V_{DD}>V_{DDA}	-	0.3	V
V_{BAT}-V_{SS}	External backup supply voltage	-0.3	5.8	V
V_{IN}	Input voltage on FT and FTf pins	V_{SS}-0.3	V_{DDIOx}+0.3	V
	Input voltage on TTa pins	V_{SS}-0.3	5.8	V
	Input voltage on any other pins	V_{SS}-0.3	5.8	V
$\lvert\triangle V_{DDx}\rvert$	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{SSx}-V_{SS}\rvert$	Variations between all the different ground pins	-	50	mV
V_{ESD}(HBM)	Electrostatic discharge voltage		3000	V

6.3 Operating conditions

6.3.1 General operating conditions

General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	48	MHz
f_{PCLK}	Internal APB clock frequency	-	0	48	MHz
V_{DD}	Standard operating voltage	-	1.8	5.5	V
V_{DDIO2}	I/O supply voltage		1.65	5.5	V
V_{DDA}	Analog operating voltage		V_{DD}	5.5	V
V_{BAT}	Backup operating voltage		2.1	5.5	V
V_{IN}	I/O input voltage	TC and RST I/O	-0.3	V_{DDIOx}+0.3	V
		TTa I/O	-0.3	V_{DDA}+0.3	
		FT and FTf I/O	-0.3	5.5	
P_D	Power dissipation at TA=85C	LQFP48	-	350	mW
		UFQFPN48	-	600	
		LQFP32		350	
		UFQFPN32		500	
		UFQFPN28		170	
		TSSOP20		250	
TA	Ambient temperature for the suffix 6 version	Maximum power dissipation	-40	85	C
		Low power dissipation	-40	105	
	Ambient temperature for the suffix 7 version	Maximum power dissipation	-40	105	C
		Low power dissipation	-40	125	
TJ	Junction temperature range	Suffix 6 version	-40	105	C
		Suffix 7 version	-40	125	

6.3.2 Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	VDD rise time rate	-	0	∞	us/V
	VDD fall time rate		20	∞	
t_{VDDA}	VDDA rise time rate	-	0	∞	
	VDDA fall time rate		20	∞	

6.3.3 Embedded reset and power control block characteristics

Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{POR/PDR}$	Power on/down reset threshold	Falling edge	1.51	1.58	1.65	V
		Rising edge	1.54	1.62	1.70	
$V_{PDRhyst}$	PDR hysteresis	-	-	40	-	mV
$t_{RSTTEMPO}$	Reset temporization	-	1.5	2.5	4.5	ms

Programmable voltage detector characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD0}	PVD threshold 0	Falling edge	1.59	1.67	1.75	V
		Rising edge	1.75	1.83	1.91	
V_{PVD1}	PVD threshold 1	Falling edge	1.75	1.83	1.91	
		Rising edge	1.90	1.98	2.06	
V_{PVD2}	PVD threshold 2	Falling edge	1.90	1.98	2.06	
		Rising edge	2.06	2.14	2.22	
V_{PVD3}	PVD threshold 3	Falling edge	2.06	2.14	2.22	
		Rising edge	2.21	2.29	2.37	
V_{PVD4}	PVD threshold 4	Falling edge	2.21	2.29	2.37	
		Rising edge	2.35	2.43	2.51	
V_{PVD5}	PVD threshold 5	Falling edge	2.35	2.43	2.51	
		Rising edge	2.49	2.57	2.65	
V_{PVD6}	PVD threshold 6	Falling edge	2.49	2.57	2.65	
		Rising edge	2.64	2.72	2.80	
V_{PVD7}	PVD threshold 7	Falling edge	2.64	2.72	2.80	
		Rising edge	2.80	2.88	2.96	
$V_{PVDhyst}$	PVD hysteresis	-	-	160	-	mV
$I_{DD(PVD)}$	PVD current consumption	-		0.15		uA

6.3.4 Embedded reference voltage

Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	-40C<TA<+105	1.22	1.23	1.24	V
t_{START}	ADC_IN17 buffer startup time	-		-	10	us
$t_{S\_vrefint}$	ADC sampling time when reading the internal reference voltage	-	8	-	-	us
$\triangle V_{REFINNT}$	Internal reference voltage spread over the temperature range	V_{DDA}=3V	-	-	10	mV
T_{Coeff}	Temperature coefficient	-	-100	-	100	ppm/C

6.3.5 Supply current characteristics

Typical current consumption (VDD+VDDA @ 3.6V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD}+I_{DDA}$	Run from Flash memory	All peripherals enabled, HSI 8MHz		3.7		mA
		All peripherals enabled, HSI48		15.0		
	Stop mode	Regulator in low-power mode, all oscillators OFF		6.2		uA
	Standby mode	Regulator in low-power mode, all oscillators OFF		6.0		uA

6.3.6 Wakeup time from low-power mode

Low-power mode wakeup timings

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{WUSTOP}	Wakeup from stop mode	Regulator in run mode	-	2.8	5	us
t_{START}		Regulator in low power mode		4.6	10	
$t_{WUSTANNDBY}$	Wakeup from standby mode	-	-	50	-	
$t_{WUSLEEP}$	Wakeup from sleep mode	-	4 SYSCLK cycles			

6.3.7 External clock source characteristics

High-speed external user clock characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{HSE_EXT}	User external clock source frequency	-	8	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage	0.7*V_{DDIOx}	-	V_{DDIOx}	V
V_{HSEL}	OSC_IN input pin low level voltage	VSS	-	0.3*V_{DDIOx}	
$t_{W(HSEH)}$ $t_{W(HSEL)}$	OSC_IN high or low time	15	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time	-	-	20	

Low-speed external user clock characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSE_EXT}	User external clock source frequency	-	32.768	1000	KHz
V_{LSEH}	OSC32_IN input pin high level voltage	0.7*V_{DDIOx}	-	V_{DDIOx}	V
V_{LSEL}	OSC32_IN input pin low level voltage	VSS	-	0.3*V_{DDIOx}	
$t_{W(LSEH)}$ $t_{W(LSEL)}$	OSC32_IN high or low time	450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time	-	-	50	

HSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	20	MHz
RF	Feedback resistor	-	-	200	-	KΩ
I_{DD}	HSE current consumption	VDD=3.3V, Rm=45Ω, CL=10pF@8MHz		0.57		mA
g_m	Oscillator transconductance	Startup	10	-	-	mA/V
$t_{SU(HSE)}$	Startup time	VDD is stabilized	-	2	-	ms

LSE oscillator characteristics (f_{LSE}=32.768KHz)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	LSE current consumption	low drive capability		360		nA
		medium-low drive capability		450		
		medium-high drive capability		540		
		high drive capability		700		
g_m	Oscillator transconductance	low drive capability	5	-	-	uA/V
		medium-low drive capability	8			
		medium-high drive capability	15			
		high drive capability	25			
$t_{SU(LSE)}$	Startup time	V_{DDIOx} is stabilized	-	2	-	s

6.3.8 Internal clock source characteristics

HSI48 oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI48}	Frequency	-		48		MHz
TRIM	HSI48 user-trimming step	-		0.15		%
DuCy	Duty cycle	-	45	-	55	%
ACC_{HSI48}	Accuracy of the HSI48 oscillator(factory calibrated)	TA=-40 to 105 @SS	-1.84		2.00	%
		TA=-40 to 105@TT	-1.58		1.76	
		TA=-40 to 105@FF	-1.24		1.72	
$t_{SU(HSI48)}$	HSI48 oscillator startup time	-			6	us
$I_{DDA(HSI48)}$	HSI48 oscillator power consumption	-		643	801	uA

LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	31.9	40	55.5	KHz
$t_{SU(LSI)}$	LSI oscillator startup time	-			100	us
$I_{DDA(LSI)}$	LSI oscillator power consumption	-		400		nA

6.3.9 PLL characteristics

PLL characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	1	8	24	MHz
t_{PLL_OUT}	PLL multiplier output clock	16		96	MHz
t_{LOCK}	PLL lock time	30		100	us
$I_{DDA(PLL)}$	PLL power consumption			350	uA
$Jitter_{PLL}$	Cycle-to-cycle jitter			300	ps

6.3.10 Memory characteristics

Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PROG}	16-bit programming time	TA=-40 to +125			20	us
t_{ERASE}	Page(1KB) erase time				10	ms
t_{ME}	Mass erase time				40	ms
I_{DD}	Supply current	Write mode			3.5	mA
		Erase mode			2	mA

N_{END}	Endurance	TA=-40 to +125	20			kcycle
t_{RET}	Data retention	TA=25C	100			Year

6.3.11 EMC characteristics

EMC characteristics

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	VDD=3.3V, LQFP48, TA=25C, f_{HCLK}=48 MHz, conforming to IEC 61000-4-2	3B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100pF on V_{DD} and V_{SS} pins to induce a functional disturbance	VDD=3.3V, LQFP48, TA=25C, f_{HCLK}=48 MHz, conforming to IEC 61000-4-4	4B

EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs.[f_{HSE}/f_{HCLK}] 8/48 MHz	Unit
SEMI	Peak level	VDD=3.6V, TA=25C, LQFP48 package compliant with IEC 61967-2	0.1 to 30MHz	-9	dBuV
			30 to 130MHz	9	
			130 MHz to 1GHz	17	
			EMI level	3	-

6.3.12 Electrical sensitivity characteristics

ESD absolute maximum ratings

Symbol	Parameter	Conditions	Packages	Class	Maxi value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	TA=+25C, conforming to JESD22-A114	All	2	3000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	TA=+25C, conforming to AEC-Q100-011	All	C6	1000	V

6.3.13 I/O current injection characteristics

I/O current injection susceptibility

Symbol	Parameter	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current	-5	+5	mA

6.3.14 I/O port characteristics

I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	TC and TTa I/O			$0.3*V_{DDIOx}$	V
		FT and FTf I/O			$0.475*V_{DDIOx}-0.2$	
		All I/Os			$0.3*V_{DDIOx}$	
V_{IH}	High level input voltage	TC and TTa I/O	$0.445*V_{DDIOx}+0.4$			V
		FT and FTf I/O	$0.5*V_{DDIOx}+0.2$			
		All I/Os	$0.7*V_{DDIOx}$			
V_{hys}	Schmitt trigger hysteresis	TC and TTa I/O		200		mV
		FT and FTf I/O		100		
I_{lkg}	Input leakage current	TC,FT and FTf I/O TTa in digital mode $V_{SS}<=V_{IN}<=V_{DDIOx}$			±0.1	uA
		TTa in digital mode $V_{DDIOx}<=V_{IN}<=V_{DDA}$			1	
		TTa in analog mode $V_{SS}<=V_{IN}<=V_{DDA}$			±0.2	
		FT and FTf I/O $V_{DDIOx}<=V_{IN}<=5V$			10	
R_{PU}	Weak pull-up resistor	$V_{IN}=V_{SS}$		40		KΩ
R_{PD}	Weak pull-down resistor	$V_{IN}=-V_{DDIOX}$		40		KΩ
C_{IO}	I/O pin capacitance			5		pF

Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage for an I/O pin	CMOS port	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin	$\|I_{IO}\|$ = 8mA V_{DDIOx}>= 2.7V	$V_{DDIOx}-0.4$	-	

V_{OL}	Output low level voltage for an I/O pin	TTL port	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin	$\|I_{IO}\|$ = 8mA V_{DDIOx}>= 2.7V	2.4	-	
V_{OL}	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 20mA V_{DDIOx}>= 2.7V	-	1.3	V
V_{OH}	Output high level voltage for an I/O pin		V_{DDIOx}-1.3	-	
V_{OL}	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 6mA V_{DDIOx}>= 2.7V	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		V_{DDIOx}-0.4	-	
V_{OL}	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 4mA V_{DDIOx}>= 2.7V	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		V_{DDIOx}-0.4	-	
V_{OLFm+}	Output low level voltage for an FTf I/O pin in FM+ mode	$\|I_{IO}\|$ = 20mA V_{DDIOx}>= 2.7V	-	0.4	V
		$\|I_{IO}\|$ = 10mA	-	0.4	

I/O AC characteristics

OSPEEDRy [1:0]	Symbol	Parameter	Conditions	Min	Max	Unit
x0	$f_{max(IO)out}$	Maximum frequency	C_L=50pF, V_{DDIOx}>=2V	-	2	MHz
	$t_{f(IO)out}$	Output fall time		-	38	ns
	$t_{r(IO)out}$	Output rise time		-	39	
01	$f_{max(IO)out}$	Maximum frequency	C_L=50pF, V_{DDIOx}>=2V	-	10	MHz
	$t_{f(IO)out}$	Output fall time		-	25	ns
	$t_{r(IO)out}$	Output rise time		-	25	
11	$f_{max(IO)out}$	Maximum frequency	C_L=30pF, V_{DDIOx}>=2.7V	-	50	MHz
			C_L=50pF, V_{DDIOx}>=2.7V	-	30	
			C_L=50pF, 2V<=V_{DDIOx}<2.7V	-	20	
	$t_{f(IO)out}$	Output fall time	C_L=30pF, V_{DDIOx}>=2.7V	-	6.5	ns
			C_L=50pF, V_{DDIOx}>=2.7V	-	9	
			C_L=50pF, 2V<=V_{DDIOx}<2.7V	-	15.5	
	$t_{r(IO)out}$	Output rise time	C_L=30pF, V_{DDIOx}>=2.7V	-	6.6	
			C_L=50pF, V_{DDIOx}>=2.7V	-	8.6	
			C_L=50pF, 2V<=V_{DDIOx}<2.7V	-	39	
Fm+ configuration	$f_{max(IO)out}$	Maximum frequency	C_L=50pF, V_{DDIOx}>=2V	-	2	MHz
	$t_{f(IO)out}$	Output fall time		-	15.5	ns
	$t_{r(IO)out}$	Output rise time		-	39	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	-	ns

6.3.15 NRST pin characteristics

NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	0.3*VDD	V
$V_{IH(NRST)}$	NRST input high level voltage	-	0.445*VDD+0.4	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up resistor	$V_{IN}=V_{SS}$	-	40	-	K Ω
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	2.7<VDD<3.6	300	-	-	ns
		2.0<VDD<3.6	500	-	-	

6.3.16 ADC characteristics

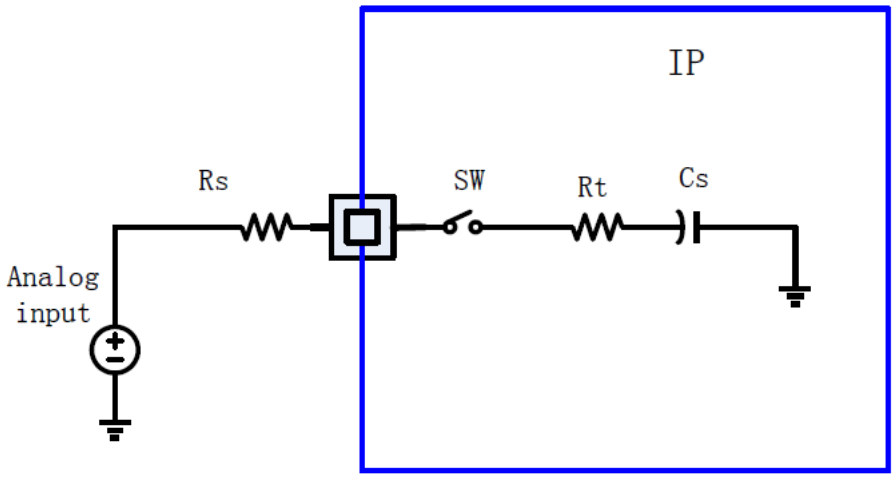
ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.8	3.3	5.5	V
$I_{DD(ADC)}$	Current consumption of the ADC	V_{DDA}=3.3V	-	1.1	-	mA
f_{ADC}	ADC clock frequency	-	-	-	16	MHz
f_S	Sampling rate	12-bit resolution	0.03	-	1	MHz
f_{TRIG}	External trigger frequency	12-bit resolution	-	-	18	$1/f_{ADC}$
V_{AIN}	Conversion voltage range		0		V_{DDA}	V
R_t	Input resistor during sampling	V_{DDA}=3V		0.5		k Ω
C_s	Internal sample and hold capacitor			26	30	pF
t_S	Sampling time	f_{ADC}=16MHz	4	-	-	$1/f_{ADC}$
t_{STAB}	Stabilization time		32	-	-	$1/f_{ADC}$
t_{CONV}	Total conversion time	12-bit resolution		12		$1/f_{ADC}$

ADC accuracy

Symbol	Parameter	Conditions	Typ	Max	Unit
ET	Total unadjusted error	f_{PCLK}=48MHz,	±1.5	-	LSB
EO	Offset error	f_{ADC}=16MHz,RAIN<10k Ω	±1.5	±3.0	
EG	Gain error	V_{DDA}=3V to 3.6V	±2	±5	
ED	Differential linearity error	TA=25C	±0.6	±1.5	
EL	Integral linearity error		±1.5	±3.0	

Analog Input Equivalent Circuit



$$Rs = \frac{Tsamp}{10 * Cs} - Rt$$

R_{AIN} max for f_{ADC} = 16 MHz

T_s(cycles)	t_s(us)	RAIN max (kΩ)
4	0.35	0.33
7.5	0.47	1.1
13.5	0.84	2.3
28.5	1.78	5.4
41.5	2.59	8.1
55.5	3.47	11.1
71.5	4.47	14.4
239.5	14.97	49.4

6.3.17 Temperature sensor characteristics

TS characteristics

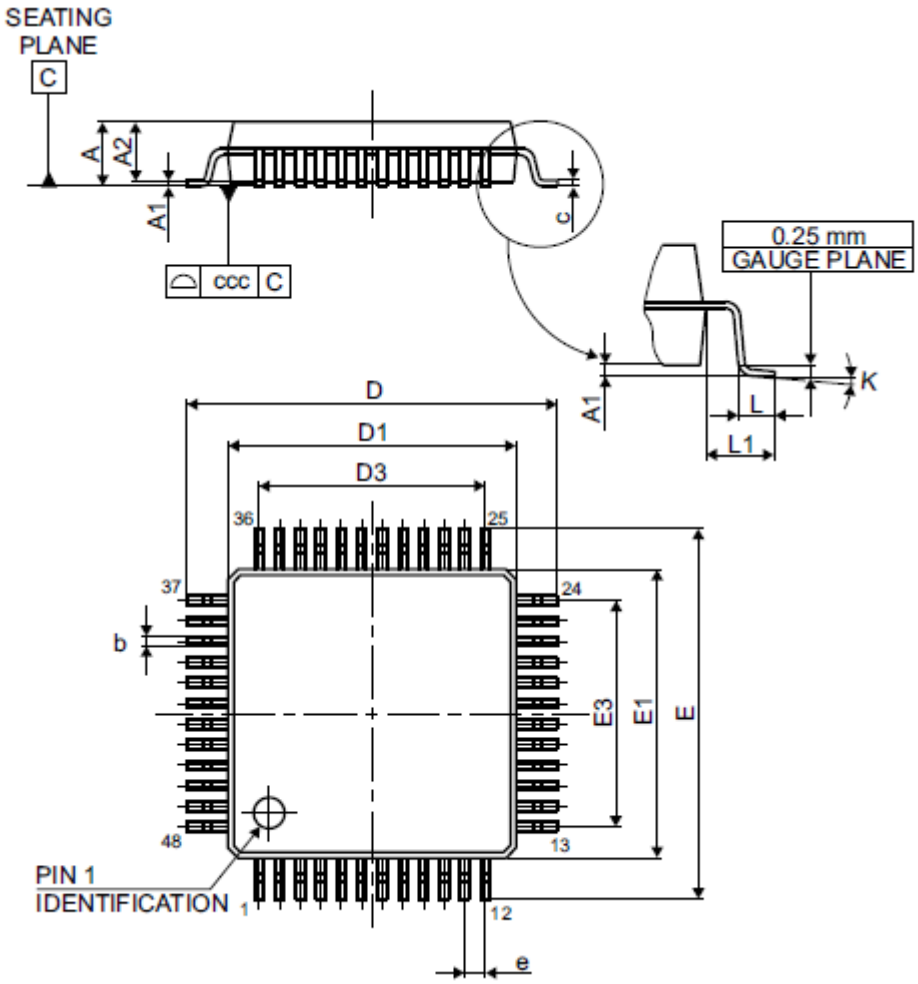
Symbol	Parameter	Min	Typ	Max	Unit
T_L	V_{SENSE} linearity with temperature	-	±1	±2	C
Avg_Slope	Average slope	4.2	4.28	4.36	mV/C
V30	Voltage at 30C	1.423	1.425	1.43	V
tSTART	ADC_IN16 buffer startup time	1	-	5	us
t_{S_temp}	ADC sampling time when reading the temperature	4	-	-	us

7 Package information

7.1 LQFP48 package information

LQFP48 is a 48-pin, 7 x 7 mm low-profile quad flat package.

LQFP48 package outline



LQFP48 package mechanical data

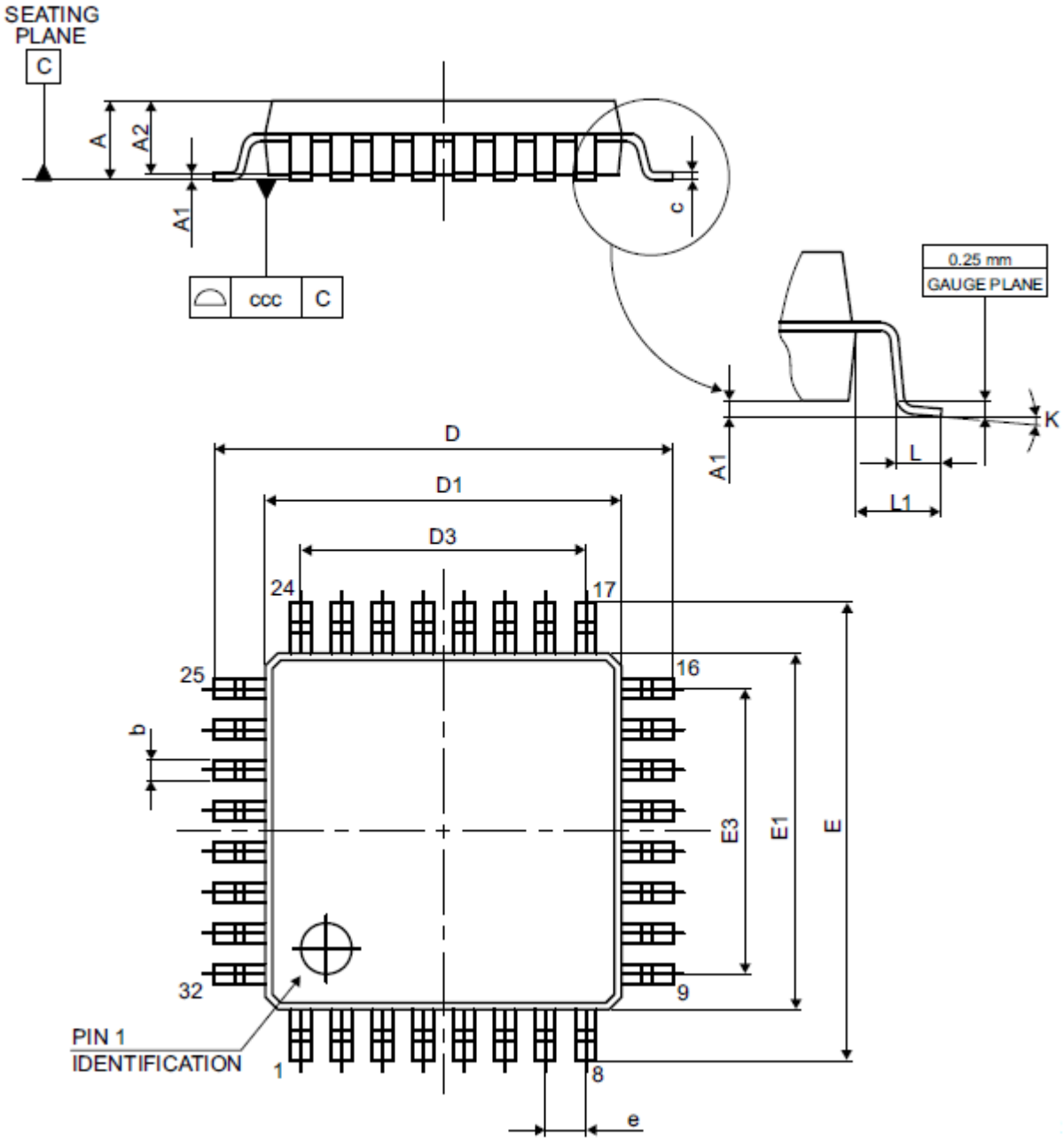
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

7.2 LQFP32 package information

LQFP32 is a 32-pin, 7 x 7 mm low-profile quad flat package.

LQFP32 package outline



LQFP32 package mechanical data

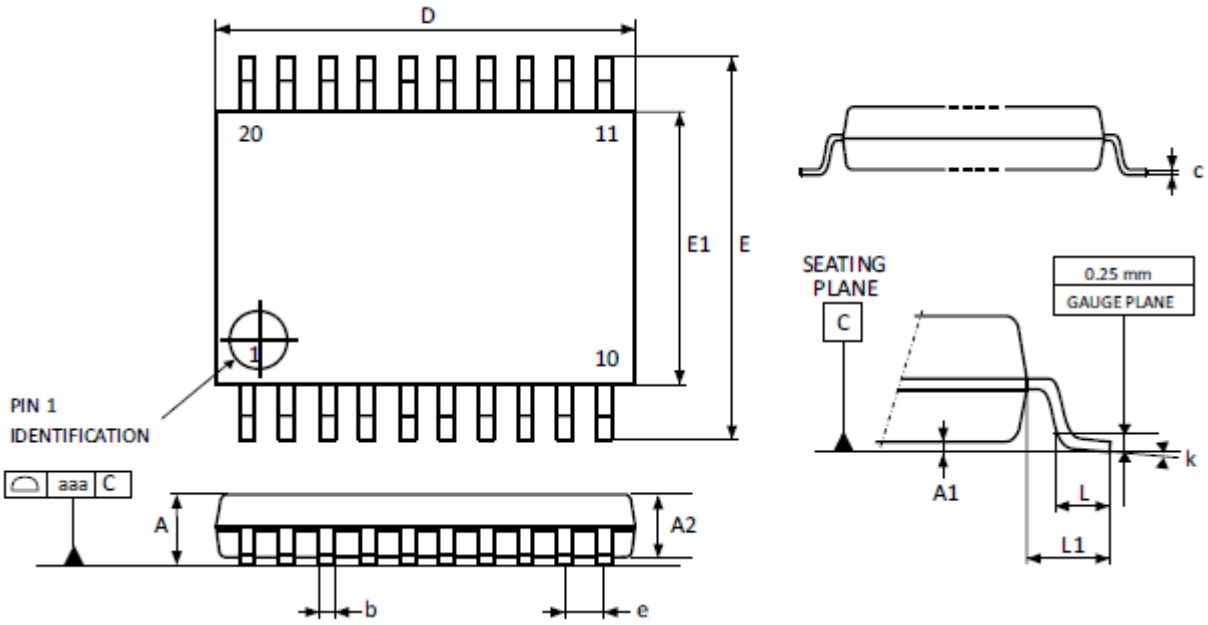
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.600	-	-	0.2205	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.600	-	-	0.2205	-
e	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.

7.3 TSSOP20 package information

TSSOP20 is a 20-lead thin shrink small-outline, 6.5 x 4.4 mm, 0.65 mm pitch, package.

TSSOP20 package outline



TSSOP20 package mechanical data

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
c	0.090	-	0.200	0.0035	-	0.0079
D[2]	6.400	6.500	6.600	0.2520	0.2559	0.2598
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1[3]	4.300	4.400	4.500	0.1693	0.1732	0.1772
e	-	0.650	-	-	0.0256	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	-	8°	0°	-	8°
aaa	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to four decimal digits.

8 Ordering information

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest FCM sales office.

Ordering information scheme

Example: FCM32 F 030 C 8 T 6 - x

Device family

FCM32 = FCM 32-bit microcontroller

Product type

F = General-purpose

H = High performance

Sub-family

030 = FCM32x030xx

Pin count

F = 20 pins

G = 28 pins

K = 32 pins

T = 36 pins

C = 48 pins

User code memory size

4 = 16 Kbyte

6 = 32 Kbyte

8 = 64 Kbyte

Package

P = TSSOP

T = LQFP

U = UFQFPN

Y = WLCSP

Temperature range

6 = -40 to 85℃

7 = -40 to 105℃

8 = -40 to 125℃

Options

x = Revision code

9 Revision history

Date	Revision	Changes
2020/1/17	0.1	Initial release
2020/4/7	0.2	Table of CH 2: SPI/USART/I2C number change to 2; RAM change to 8KB; Add register map at CH 5; Add electronical characteristics at CH 6
2020/4/8	0.21	Fix error of 6.3.8 LSI $I_{DDA(LSI)}$ unit to nA
2020/5/21	0.22	Change SPI number to 2
2020/7/15	0.23	Add V_{REFINT} min/max value Change SPI number to 1 for device with pin number < =32 Add index
2020/8/26	0.24	Add package information
2020/9/8	0.25	Add pin description and ordering information
2020/11/1	0.26	Remove 64-PIN info; 6.3.10 t_{ERASE} change from 5ms to 10ms
2020/11/25	0.27	Add TIM15
2020/11/26	0.28	6.3.16 Add RAIN max table

10 Others