FCM32F072x8/xB Datasheet

Ver 0.11

Type	Chip Revision	Mark
F072C8	C	
F072CB		
F072R8		
F072RB		

ARM®-based 32-bit MCU, up to 128KB Flash, 16KB SRAM, USB 2.0 FS Device, exCAN, 9 timers, ADC/COMP/DAC & comm. interfaces, 1.8-5.5V

Features

- ARM® 32-bit Cortex-M0 CPU， frequency up to 72 MHz
- Memories
  - ✧ 64/128 KB of Flash memory
  - ✧ FLASH speed up to 24MHz， FLASH latency can be set follow this spec
  - ✧ 16 KB SRAM
- CRC calculation unit
- ***HAU hardware arithmetic unit, supports 32 bit division and 32 bit square root operation***
- ***PLib (Private Library), protect important code can't be readout***
- Reset and power management
  - ✧ Digital and I/Os supply: V_{DD} = 1.8 - 5.5V
  - ✧ Analog supply: V_{DDA} = 1.8 - 5.5V
  - ✧ Power-on/Power down reset(POR/PDR)
  - ✧ Programmable voltage detector(PVD)
  - ✧ Low power modes: Sleep, Stop, Standby
- Clock management
  - ✧ 4 to 20 MHz crystal oscillator
  - ✧ 32 kHz oscillator for RTC with calibration
  - ✧ Internal 48 MHz RC oscillator, and divide to 8MHz
  - ✧ Internal 40 KHz RC oscillator
  - ✧ PLL use for CPU
- Up to 56 fast I/Os
  - ✧ All mappable on external interrupt vectors
  - ✧ With 5V tolerant capability when power supply is 3V, except the ADC pins
  - ✧ 14 I/Os with independent supply V_{DDIO2}
  - ✧ USB DP/DM supply from V_{DD}
- 1 DMA controller, 7channels
- One 12-bit, 1.0 us ADC(up to 16 channels)
  - ✧ Conversion range: 0 to 5.5 V
  - ✧ Embedded temp sensor
- 2 Analog Comparators
- One 12-bit DAC with 2 Channels
- Up to 18 capacitive sensing channels for touchkey, linear and rotary touch sensors
- Calendar RTC with alarm and periodic wakeup from Stop/Standby
- 12 timers
  - ✧ One 16-bit advanced-control timer for six channel PWM output
  - ✧ One 32-bit and seven 16-bit timers, with up to four IC/OC,OCN, usable for IR control decoding
  - ✧ Independent and system watchdog timers
  - ✧ ***PWM can support PLLCLK*2 as timer input clock***
  - ✧ SysTick timer
- Communication interfaces

- ✧ Two I^2C interface supporting Fast Mode Plus(1Mbit/s) with 20mA current sink, SMBus/PMBus and wakeup
- ✧ Four USARTs supporting master synchronous SPI and modem control, one with ISO7816 interface LIN, IrDA, auto baud rate detection and wakeup feature
- ✧ Two SPIs(36 Mbit/s) with 4 to 16 programmable bit frames, one with I^2S interface multiplexed
- ✧ ***SPI2 support full-duplex I2S, combo with I2S2 and I2S2EXT***
- ✧ ***One bxCAN***
- ✧ ***USB 2.0 full-speed Device. Device able to run from internal 48MHz oscillator and with BCD and LPM support***
- ✧ ***LED Light Strip Interface(LLSI), can drive 7 LED strips***

- HDMI CEC, wakeup on header reception
- Debug mode
  - ✧ Serial wire debug(SWD)
- 96-bit unique ID
- Packages
  - ✧ LQFP48
  - ✧ UFQFPN48
  - ✧ LQFP64

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1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the FCM32F072 microcontrollers.

For information on the arm Cortex-M0 core, please refer to the Cortex-M0 Technical Reference Manual, available from the www.arm.com website.

2 Description

The FCM32F072 microcontrollers incorporate the high-performance arm Cortex-M0 32-bit RISC core operating at up to 72 MHz frequency, high-speed embedded memories (up to 128 Kbytes of Flash memory and 16 Kbytes of SRAM), and an extensive range of enhanced peripherals and I/Os. All devices offer standard communication interfaces (I^2C, SPI/I^2S, HDMI-CEC and USARTs), one USB Full-speed Device (crystal-less), bxCAN, 12-bit ADC/DAC, COMP, seven 16-bit timers, one 32-bit timer and an advanced-control PWM timer.

The FCM32F072 microcontrollers operate in the -40 to +85C temperature ranges, from a 1.8 to 5.5 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

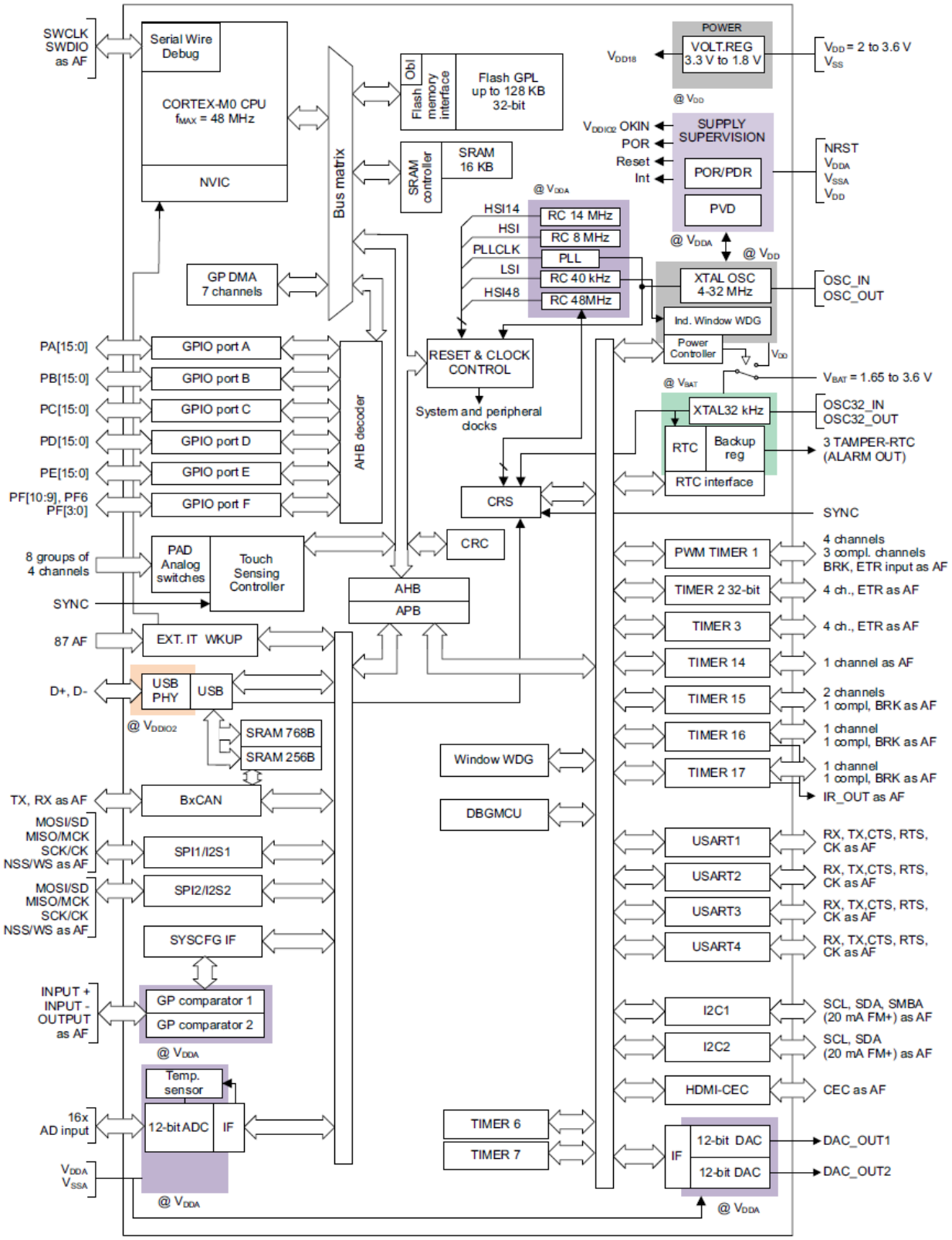
The FCM32F072 microcontrollers include devices in several different packages ranging from 48 pins to 64 pins with a die form also available upon request. Depending on the device chosen, different sets of peripherals are included.

These features make the FCM32F072 microcontrollers suitable for a wide range of applications such as application control and user interfaces, hand-held equipment, A/V receivers and digital TV, PC peripherals, gaming and GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms and HVACs.

FCM32F072 device features and peripheral counts

Part No.	Frequency (MHz)	Flash (KB)	SRAM (KB)	GPIO	16bit Timer	32bit Timer	SysTick Timer	WDG	RTC	ADC Engine	ADC Channel	DAC Channel	OPAMP	COMP	TSC Channel	SPI	I2S	I2C	U(S)ART	CEC	USBD	USBHD	USBHUB	bxCAN	exCAN	HAU	LLSI Channel	PLib	Package
FCM32F072C8T6	72	64	16	37	8	1	1	2	1	1	13	2	-	2	16	2	2	2	4	1	1	-	-	1	-	1	7	√	LQFP48
FCM32F072C8U6	72	64	16	37	8	1	1	2	1	1	13	2	-	2	16	2	2	2	4	1	1	-	-	1	-	1	7	√	QFN48
FCM32F072CBT6	72	128	16	37	8	1	1	2	1	1	13	2	-	2	16	2	2	2	4	1	1	-	-	1	-	1	7	√	LQFP48
FCM32F072CBU6	72	128	16	37	8	1	1	2	1	1	13	2	-	2	16	2	2	2	4	1	1	-	-	1	-	1	7	√	QFN48
FCM32F072R8T6	72	64	16	51	8	1	1	2	1	1	19	2	-	2	17	2	2	2	4	1	1	-	-	1	-	1	7	√	LQFP64
FCM32F072RBT6	72	16	16	51	8	1	1	2	1	1	19	2	-	2	17	2	2	2	4	1	1	-	-	1	-	1	7	√	LQFP64

Block diagram



3 Functional overview

3.1 ARM® Cortex-M0 core

ARM® Cortex-M0 is a generation of arm 32-bit RISC processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.
The ARM® Cortex-M0 processors feature exceptional code-efficiency, delivering the high performance expected from an arm core, with memory sizes usually associated with 8- and 16-bit devices.
The FCM32F072 devices embed arm core and are compatible with all arm tools and software.

3.2 Memories

The device has he following features:

- 16 KB of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states and featuring embedded parity checking with exception generation for fail-critical applications.
- The non-volatile memory is divided into two arrays:
  - 64/128 KB of embedded Flash memory for programs and data
  - Option Bytes

The option bytes are used to write-protect the memory (with 4 KB granularity) and/or readout-protect the whole memory with the following options:

- Level 0: no readout protection
- Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
- Level 2: chip readout protection, debug features(SWD) and boot in RAM selection disabled

3.3 Boot modes

At startup, the boot pin and boot selector option bits are used to select one of the three boot options:

- Boot from User Flash memory
- Boot from System Memory
- Boot from embedded SRAM

The boot pin is shared with the standard GPIO and can be disabled through the boot selector option bits.
The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART on pins PA9/PA10.

3.4 Cyclic redundancy check calculation and Hardware arithmetic unit (CRC & HAU)

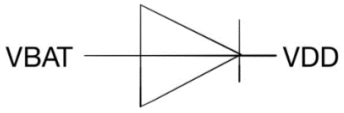
The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a CRC-32 (Ethernet) polynomial.
Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

HAU can calculate 32-bit division and 32-bit square root.

3.5 Power management

3.5.1 Power supply

- V_{DD} = 1.8 - 5.5V: external power supply for I/Os and the internal regulator. It is provided externally through VDD pins.
- V_{DDA} = 1.8 - 5.5V: external analog power supply for ADC, Reset blocks, RCs and PLL. It is provided externally through VDDA pin. The VDDA voltage level must be always greater or equal to the VDD voltage level and must be established first.
- V_{DDIO2} = 1.8 - 5.5V: external power supply for marked I/Os. The VDDIO2 voltage level is completely independent from VDD or VDDA, but it must not be provided without a valid supply on VDD. The VDDIO2 supply is monitored and compared with the internal reference voltage (VREFINT). When the VDDIO2 is below this threshold, all the I/Os supplied from this rail and it can be used to generate an interrupt.
- VBAT = 1.8 – 5.5V: The other optional power supply. Power supply for VDD (through internal DIODE) when VDD is not present.



3.5.2 Power supply supervisors

The device has integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 1.8 V. The device remains in reset mode when the monitored supply voltage is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

- The POR monitors only the VDD supply voltage. During the startup phase it is required that VDDA should arrive first and be greater than or equal to VDD.
- The PDR monitors both the VDD and VDDA supply voltages, however the VDDA power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that VDDA is higher than or equal to VDD.

The device features an embedded programmable voltage detector (PVD) that monitors the VDD power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when VDD drops below the V_{PVD} threshold and/or when VDD is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.5.3 Voltage regulator

The regulator has two operating modes and it is always enabled after reset.

- Main (MR) is used in normal operating mode (RUN)
- Low power (LPR) can be used in Stop mode where the power demand is reduced.

In Standby mode, it is put in LPR mode. In this mode, MCU core and SRAM, SFRs and most peripherals stopped, the contents of the registers and SRAM are not lost.

3.5.4 Low-power modes

The FCM32F072 microcontrollers support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- Sleep mode
  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- Stop mode
  Stop mode achieves very low power consumption while retaining the content of SRAM and registers. All clocks in the 1.5 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.
  The device can be woken up from Stop mode by any of the EXTI lines. The EXTI line source can be one of the 16 external lines, the PVD output, RTC, I2C1, USART1, USB or the CEC.
  The CEC, USART1 and I2C1 peripherals can be configured to enable the HSI RC oscillator so as to get clock for processing incoming data. If this is used when the voltage regulator is put in low power mode, the regulator is first switched to normal mode before the clock is provided to the given peripheral.
- Standby mode
  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator enter LPR mode. PLL, the HSI RC and the HSE crystal oscillators are also switched off. The content of SRAM and registers are retained.
  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pins, or an RTC event occurs.

Note： The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

3.6 Clocks and startup

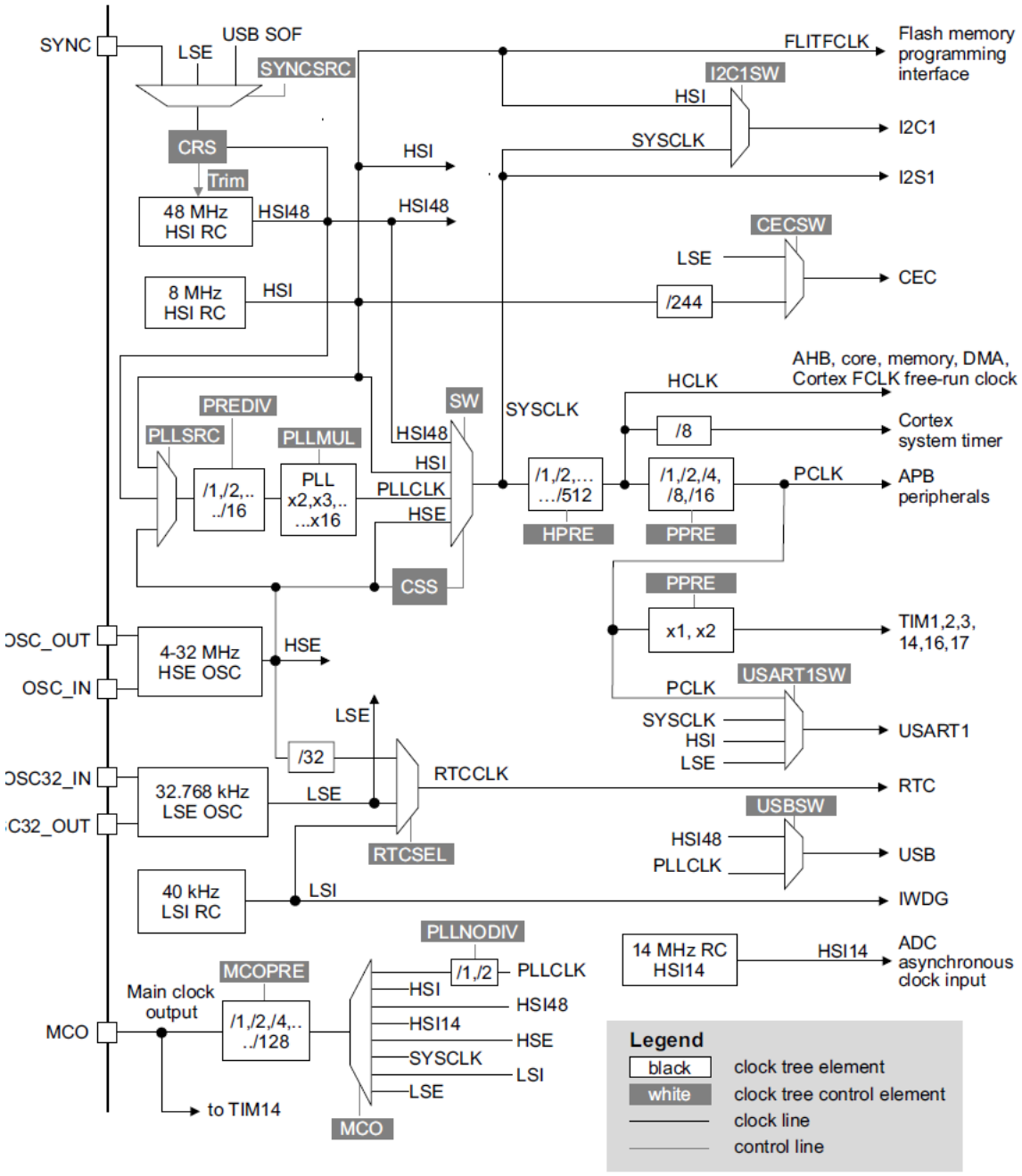
System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-20 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the application to configure the frequency of the AHB and the APB domains.

The maximum frequency of the AHB and APB domains is 72 MHz.

Additionally, also the internal RC 48 MHz oscillator can be selected for system clock or PLL input source. This oscillator can be automatically fine-trimmed by the means of the CRS peripheral using the external synchronization.

Clock tree



3.7 GPIO

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

The I/O configuration can be locked if needed following a specific sequence in order to avoid spurious

writing to the I/Os registers.

3.8 Direct memory access controller (DMA)

The 7 channel general-purpose DMAs manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers.
The DMA supports circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.
Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.
DMA can be used with the main peripherals: SPIx, I2Sx, I2Cx, USARTx, all TIMx timers (except TIM14) and ADC, DAC.

3.9 Interrupts and events

3.9.1 Nested vectored interrupt controller (NVIC)

The FCM32F072 family embeds a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels (not including the 16 interrupt lines of Cortex-M0) and 4 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.9.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 24 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect and external line with a pulse width shorter than the internal clock period. Up to 38 GPIOs can be connected to the 16 external lines.

3.9.3 Interrupt Vectors

		Type of priority	Acronym	Description	Address
-	-	-	-	Reserved	0x0000 0000

-	-3	Fixed	Reset	Reset	0x0000 0004
-	-2	Fixed	NMI	Non maskable interrupt (CSS linked.)	0x0000 0008
-	-1	Fixed	HardFault	All class of fault	0x0000 000C
-	3	Settable	SVCall	System service call via SWI instruction	0x0000 002C
-	5	Settable	PendSV	Pendable request for system service	0x0000 0038
-	6	Settable	SysTick	System tick timer	0x0000 003C
0	7	Settable	WWDG	Window watchdog interrupt	0x0000 0040
1	8	Settable	PVD_VDDIO2	PVD and VDDIO2 supply comparator interrupt (combined EXTI lines 16 and 31)	0x0000 0044
2	9	Settable	RTC	RTC interrupts (combined EXTI lines 17,19 and 20)	0x0000 0048
3	10	Settable	FLASH	Flash global interrupt	0x0000 004C
4	11	Settable	RCC_CRS	RCC and CRS global interrupts	0x0000 0050
5	12	Settable	EXTI0_1	EXTI line[1:0] interrupts	0x0000 0054
6	13	Settable	EXTI2_3	EXTI Line[3:2] interrupts	0x0000 0058
7	14	Settable	EXTI4_15	EXTI line[15:4] interrupts	0x0000 005C
8	15	Settable	TSC	Touch sensing interrupt	0x0000 0060
9	16	Settable	DMA_CH1	DMA channel 1 interrupt	0x0000 0064
10	17	Settable	DMA_CH2_3 DMA2_CH1_2	DMA channel 2 and 3 interrupts DMA2 channel 1 and 2 interrupts	0x0000 0068
11	18	Settable	DMA_CH4_5_6_7 DMA2_CH3_4_5	DMA channel 4,5,6 and 7 interrupts DMA2 channel 3,4 and 5 interrupts	0x0000 006C
12	19	Settable	ADC_COMP	ADC and COMP interrupts (ADC interrupt combined with EXTI lines 21 and 22)	0x0000 0070
13	20	Settable	TIM1_BRK_UP_ TRG_COM	TIM1 break, update, trigger and commutation interrupts	0x0000 0074
14	21	Settable	TIM1_CC	TIM1 capture compare interrupts	0x0000 0078
15	22	Settable	TIM2	TIM2 global interrupt	0x0000 007C
16	23	Settable	TIM3	TIM3 global interrupt	0x0000 0080
17	24	Settable	TIM6_DAC	TIM6 global interrupt and DAC underrun interrupt	0x0000 0084
18	25	Settable	TIM7	TIM7 global interrupt	0x0000 0088
19	26	Settable	TIM14	TIM14 global interrupt	0x0000 008C
20	27	Settable	TIM15	TIM15 global interrupt	0x0000 0090
21	28	Settable	TIM16	TIM16 global interrupt	0x0000 0094
22	29	Settable	TIM17	TIM17 global interrupt	0x0000 0098
23	30	Settable	I2C1	I2C1 global interrupt (combined with EXTI line 23)	0x0000 009C
24	31	Settable	I2C2	I2C2 global interrupt	0x0000 00A0
25	32	Settable	SPI1	SPI1 global interrupt	0x0000 00A4
26	33	Settable	SPI2_***LLSI***	SPI2 and LLSI global interrupt	0x0000 00A8
27	34	Settable	USART1	USART1 global interrupt (combined with EXTI line 25)	0x0000 00AC
28	35	Settable	USART2	USART2 global interrupt (combined with EXTI line 26)	0x0000 00B0
29	36	Settable	USART3_4_5_6_7_8	USART3, 4, 5, 6, 7 and 8 global interrupts (combined with EXTI line 28)	0x0000 00B4
30	37	Settable	CEC_CAN_***USBHUB***	CEC, CAN1/2, and ***USBHUB*** interrupts	0x0000 00B8
31	38	Settable	USB	USBD or ***USBHD*** global interrupt(combined with EXTI line 18)	0x0000 00BC

3.10 Analog-to-digital converter (ADC)

The 12-bit analog-to-digital converter has up to 10 external and 3 internal (temperature sensor, voltage reference, VBAT voltage measurement) channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.
The ADC can be served by the DMA controller.
An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

3.10.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.
The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.
The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.
To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by FCM. The temperature sensor factory calibration data are stored by FCM in the system memory area, accessible in read-only modes.

Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at a temperature of 30C(+/-5C), VDDA = 3.3V	0x1FFFF7B8-0x1FFFF7B9
TS_CAL2	TS ADC raw data acquired at a temperature of 11)C(+/-5C), VDDA = 3.3V	0x1FFFF7C2-0x1FFFF7C3

3.10.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC. V_{REFINT} is internally connected to the ADC_IN17 input channel. The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Internal voltage reference calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at a temperature of 30C(+/-5C), VDDA = 3.3V	0x1FFFF7BA-0x1FFFF7BB

3.10.3 V_{BAT} battery voltage monitoring

The embedded hardware feature allows the application to measure the VBAT battery voltage using the internal ADC channel ADC_IN18. As the VBAT voltage may be higher than VDDA, and thus outside the ADC input range, the VBAT pin is internally connected to a bridge divider by 2. As a consequence, the

converted digital value is half of the VBAT voltage.

3.11 Digital-to-analog Convertor (DAC)

The two 12-bit buffered DAC channels can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in non-inverting configuration.

This digital interface supports the following features:

- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion

Six DAC trigger inputs are used in the device. The DAC is triggered through the timer trigger outputs and the DAC interface is generating its own DMA requests.

3.12 Comparators (COMP)

The device embeds two fast rail-to-rail low-power comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low power) and with selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output pins
- Internal reference voltage or submultiple (1/4, 1/2, 3/4).

Both comparators can wakeup from STOP mode, generate interrupts and breaks for the timers and can be also combined into a window comparator.

3.13 Touch sensing controller (TSC)

The FCM32F072 devices provides a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 16 capacitive sensing channels distributed over 6 analog I/O groups. Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic…). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists in charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage, this acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate. For operation one capacitive sensing GPIO in each group is connected to an external capacitor and cannot be used as effective touch sensing channel.

Capacitive sensing GPIOs available on FCM32F072 devices

Group	Capacitive sensing signal name	Pin name
1	TSC_G1_IO1	PA0

Group	Capacitive sensing signal name	Pin name
4	TSC_G4_IO1	PA9

	TSC_G1_IO2	PA1
	TSC_G1_IO3	PA2
	TSC_G1_IO4	PA3
2	TSC_G2_IO1	PA4
	TSC_G2_IO2	PA5
	TSC_G2_IO3	PA6
	TSC_G2_IO4	PA7
3	TSC_G3_IO1	PC5
	TSC_G3_IO2	PB0
	TSC_G3_IO3	PB1
	TSC_G3_IO4	PB2

	TSC_G4_IO2	PA10
	TSC_G4_IO3	PA11
	TSC_G4_IO4	PA12
5	TSC_G5_IO1	PB3
	TSC_G5_IO2	PB4
	TSC_G5_IO3	PB6
	TSC_G5_IO4	PB7
6	TSC_G6_IO1	PB11
	TSC_G6_IO2	PB12
	TSC_G6_IO3	PB13
	TSC_G6_IO4	PB14

3.14 Timers and watchdogs

The FCM32F072 devices include up to seven general-purpose timers and an advanced control timer.

Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Maximum Operating frequency	Prescaler factor	DMA request generation	CCP channels	Complementary outputs
Advanced control	TIM1	16-bit	Up, down, Up/down	*144 MHz*	1~65536	Yes	4	Yes
General purpose	TIM2	32-bit	Up, down, Up/down	*144 MHz*	1~65536	Yes	4	No
	TIM3	16-bit	Up, down, Up/down	*144 MHz*	1~65536	Yes	4	No
	TIM14	16-bit	Up	72 MHz	1~65536	No	1	No
	TIM15	16-bit	Up	72 MHz	1~65536	Yes	2	No
	TIM16, TIM17	16-bit	Up	72 MHz	1~65536	Yes	1	Yes
Basic	TIM6 TIM7	16-bit	Up	72 MHz	1~65536	Yes	0	No

TIM1/2/3 can select 2*PLLCLK as clock for the higher PWM frequency and accuracy, achieved by TIM1SW bits of RCC->CFGR3. When 2*PLLCLK is selected, SYSCLK/HCLK/PCLK must be the same frequency and can't be any divider.
RCC_CFGR3
Address: 0x30
Reset value: 0x0000 0000
Bit9 : TIM1SW, 1=Select 2x PLLCLK as timer clock source
Bit24: TIM2SW, 1=Select 2x PLLCLK as timer clock source
Bit25: TIM3SW, 1=Select 2x PLLCLK as timer clock source

3.14.1 Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on six channels. It

has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).
The counter can be frozen in debug mode.
Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers via the Timer Link feature for synchronization of event chaining.

3.14.2 General-purpose timers (TIM2/3/14/15/16/17)

There are six synchronizable general-purpose timers embedded in the FCM32F072 devices. Each general-purpose timer can be used to generate PWM outputs, or as simple time base.

TIM2/3
FCM32F072 devices feature two synchronizable 4-channel general-purpose timers. TIM2 is based on a 32-bit auto-reload up/down counter and a 16-bit prescaler. TIM3 is based on 1 16-bit auto-reload up/down counter and a 16-bit prescaler. They feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.
The TIM2 and TIM3 general-purpose timers can work together or with the TIM1 advanced-control timer via the Timer Link feature for synchronization of event chaining.
TIM2 and TIM3 both have independent DMA request generation.
These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.
Their counters can be frozen in debug mode.

TIM14
This timer is based on a 16-bit auto-reload up counter and a 16-bit prescaler.
TIM14 features one single channel for input capture/output compare, PWM or one-pulse mode output.
Its counter can be frozen in debug mode.

TIM15/16/17
Both timers are based on a 16-bit auto-reload up counter and a 16-bit prescaler.
They each have a single channel for input capture/output compare, PWM or one-pulse mode output.
They have a complementary output with dead-time generation and independent DMA request generation.
Their counters can be frozen in debug mode.

3.14.3 Basic timers TIM6/7

TIM6/7 be used as generic 16-bit time bases.

3.14.4 Independent watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 12-bit down counter with user-defined refresh window. It is clocked from an independent 40 KHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.14.5 System window watchdog (WWDG)

The system window watchdog is based on a 7-bit down counter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PLCLK). It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.14.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source (HCLK or HCLK/8)

3.15 Real-time clock (RTC) and backup registers

The backup registers are five 32-bit registers used to store 20 bytes of user application data. They are not reset by a system or power reset, or at wake up from Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

- Calendar with subseconds, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- Automatic correction for 28, 29 (leap year), 30, and 31 day of the month
- Programmable alarm with wakeup from Stop and Standby mode capability
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize the RTC with a master clock
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy
- Two anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision

The RTC clock sources can be:

- A 32768 Hz external crystal

- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32

3.16 Inter-integrated circuit interface (I^2C)

The I^2C interface can operate in multimaster or slave modes. It can support Standard mode (up to 100 kbit/s), Fast mode (up to 400 kbit/s) and Fast Mode Plus (up to 1Mbit/s) with 20mA output drive.
They supports 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (two addresses, one with configurable mask). It also includes programmable analog and digital noise filters.
In addition, I2C1 provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. I2C1 also has a clock domain independent from the CPU clock, allowing the I2C1 to wake up the MCU from Stop mode on address match.
The I2C peripherals can be served by the DMA controller.

FCM32F072 I^2C implementation

I^2C features	I^2C1	I^2C2
7-bit addressing mode	Y	Y
10-bit addressing mode	Y	Y
Standard mode (up to 100 kbit/s)	Y	Y
Fast mode (up to 400 kbit/s)	Y	Y
Fast Mode Plus with 20mA output drive I/Os (up to 1Mbit/s)	Y	Y
Independent clock	Y	-
SMBus	Y	-
Wakeup from STOP	Y	-

3.17 Universal synchronous / asynchronous receiver / transmitter (USART)

The device embeds two universal synchronous/asynchronous receivers/transmitters (USART1, USART2) which communicate at speeds up to 12.5 Mbit/s.
They provide hardware management of the CTS, RTS and RS485 DE signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. USART1 supports also SmartCard communication (ISO7816), IrDA SIR ENDEC, LIN Master/Slave capability and auto baud rate feature, and has a clock domain independent to the CPU clock, allowing to wake up the MCU from Stop mode.
The USART interfaces can be served by the DMA controller.

FCM32F072 USART implementation

USART modes/ features	USART1/2/3	USART4
Hardware flow control for modem	Y	Y
Continuous communication using DMA	Y	Y
Multiprocessor communication	Y	Y
Synchronous mode	Y	Y
Smartcard mode	Y	-
Single-wire half-duplex communication	Y	Y

IrDA SIR ENDEC block	Y	-
LIN mode	Y	-
Dual clock domain and wakeup from Stop mode	Y	-
Receiver timeout interrupt	Y	-
Modbus communication	Y	-
Auto baud rate detection	Y	-
Driver Enable	Y	Y

3.18 Serial peripheral interface (SPI) / Inter-integrated sound interface (I^2S)

Up to two SPIs are able to communicate up to 36 Mbit/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.
Two standard I^2S interface (multiplexed with SPI) supporting four different audio standards can operate as master or slave at half-duplex communication mode. It can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by an 8-bit programmable linear prescaler. When operating in master mode, it can output a clock for an external audio component at 256 times the sampling frequency.

FCM32F072 SPI/I^2S implementation

SPI features	SPI1	SPI2
Hardware CRC calculation	Y	Y
Rx/Tx FIFO	Y	Y
NSS pulse mode	Y	Y
I^2S mode	Y	Y
I^2S Full-duplex mode	-	Y
TI mode	Y	Y

3.19 High-definition multimedia interface (HDMI) – consumer electronics control (CEC)

The device embeds a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).
This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI-CEC controller to wake up the MCU from Stop mode on data reception.

3.20 Basic controller area network (bxCAN)

The one CAN are compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. They can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit

identifiers. Each CAN has three transmit mailboxes, two receive FIFOs with 3 stages and 28 shared scalable filter banks (all of them can be used even if one CAN is used). The 256 bytes of SRAM which are allocated for each CAN (512 bytes in total) are not shared with any other peripheral.

3.21 USB FS Device (USBD)

The FCM32F072 embeds a full-speed USB device peripheral compliant with the USB specification version 2.0. The internal USB PHY supports USB FS signaling, embedded DP pull-up and also battery charging detection according to Battery Charging Specification Revision 1.2. The USB interface implements a full-speed (12 Mbit/s) function interface with added support for USB 2.0 Link Power Management. It has software-configurable endpoint setting with packet memory up-to 2 KB and suspend/resume support. It requires a precise 48 MH clock which can be generated from the internal 48 MHz oscillator in automatic trimming mode. The synchronization for this oscillator can be taken from the USB data stream itself (SOF signalization_ which allows crystal-less operation.

3.22 LED light strip interface (LLSI)

LLSI is use to easy drive RGB LED strip, up to 7 channels.

3.23 Clock recovery system (CRS)

The FCM32F072 embeds a special block which allows automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range This automatic trimming is based on the external synchronization signal, which could be either derived from USB SOF signalization, from LSE oscillator, from an external signal on CRS_SYNC pin or generated by user software. For faster lock-in during startup it is also possible to combine automatic trimming with manual trimming action.

3.24 Private LIB (PLIB)

The PLIB module can protect the code or data in a specified address range, the protected context can’t be read out from the data bus of MCU core.

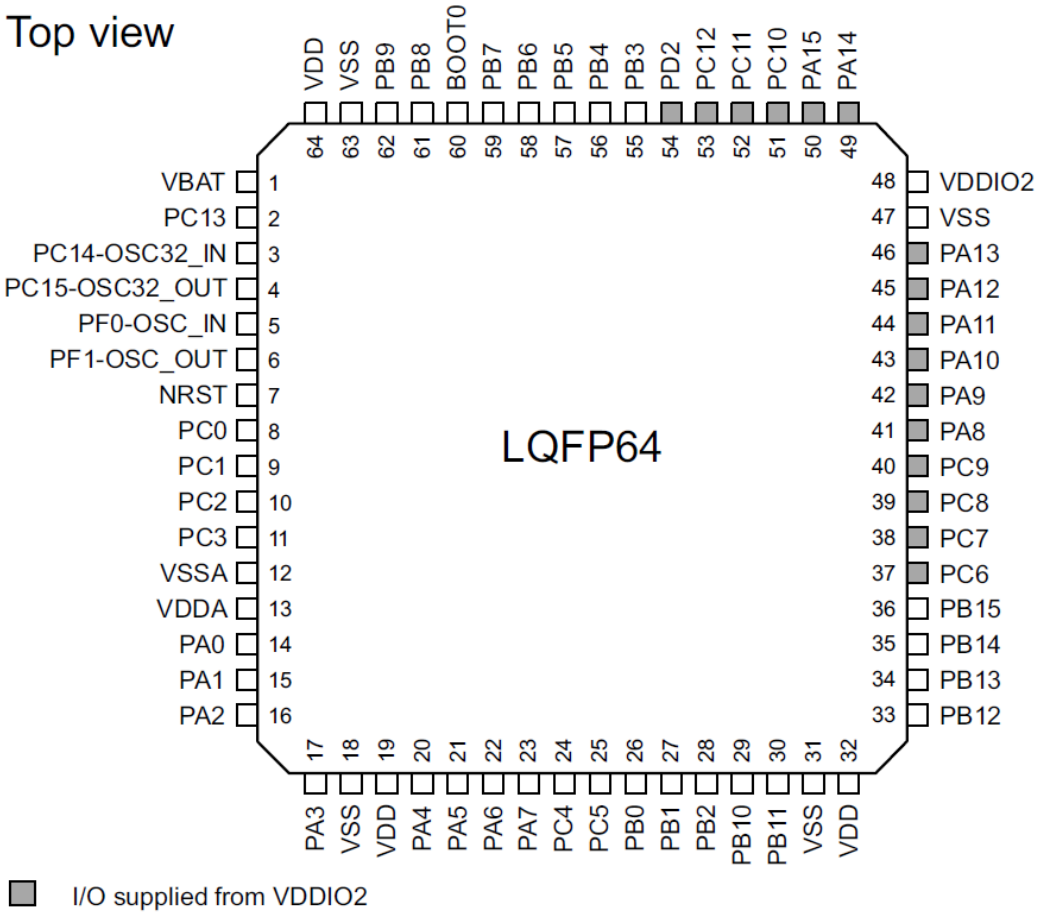
3.25 Serial wire debug port (SWJ-DP)

An ARM SWJ-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

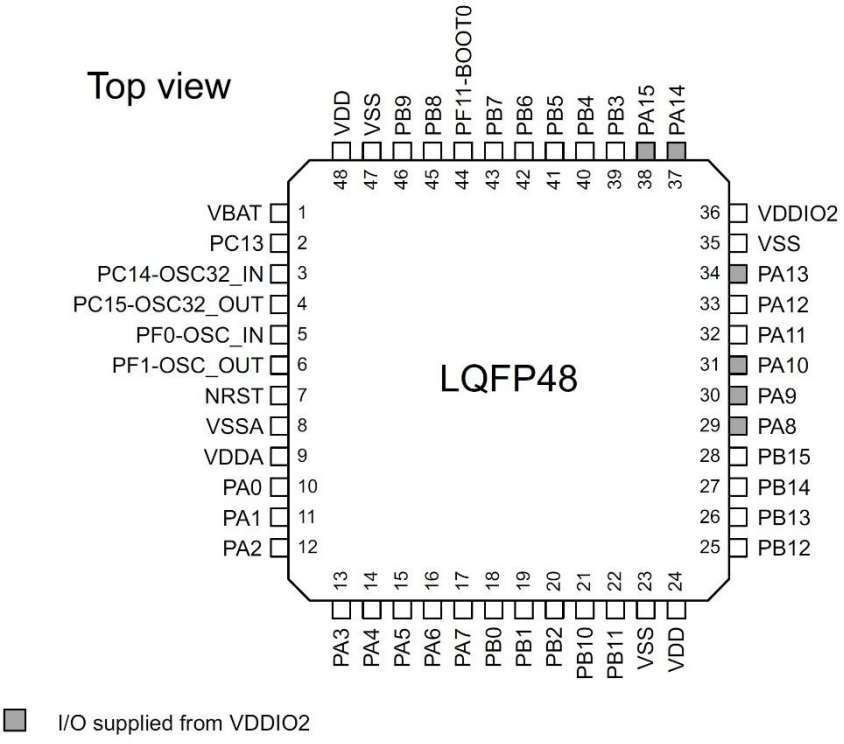
4 Pinouts and pin descriptions

Note：PA12/PA11 supplied from VDD

FCM32F072 LQFP64 pinout

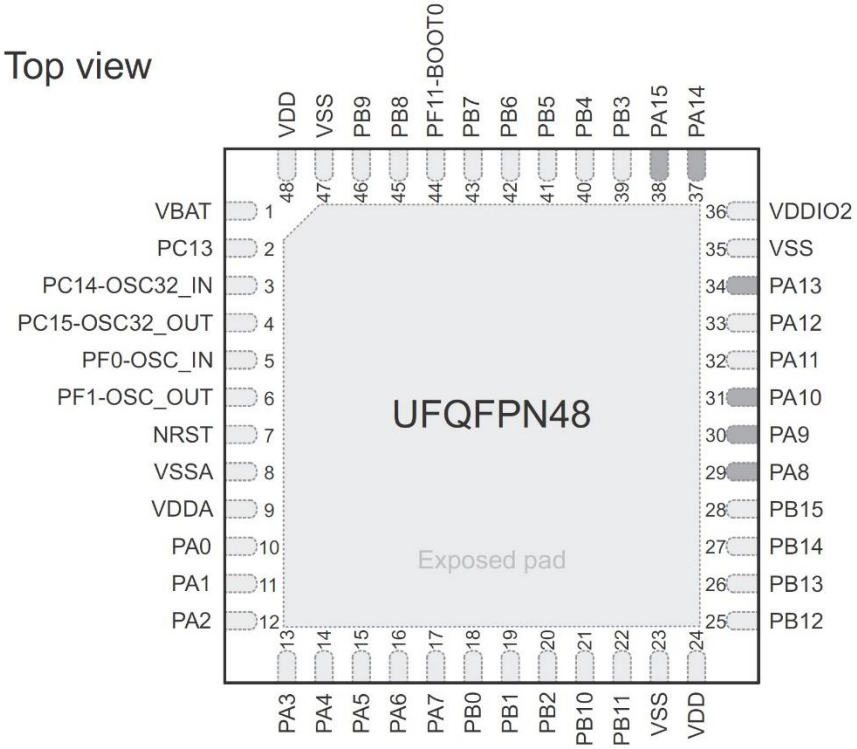


FCM32F072 LQFP48 pinout



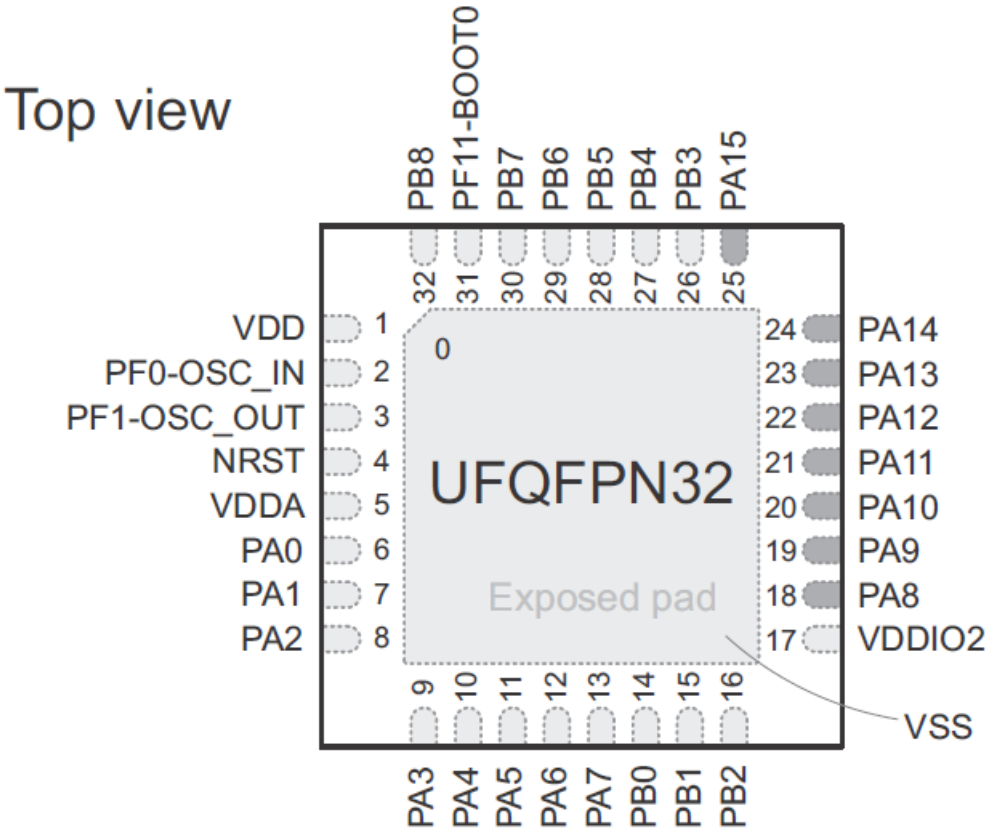
I/O supplied from VDDIO2

FCM32F072 UFQFPN48 pinout



I/O supplied from VDDIO2

FCM32F072 UFQFPN32 pinout



Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I/O	Input / output pin
I/O structure		FT	5 V-tolerant I/O
		FTf	5 V-tolerant I/O, FM+ capable
		TTa	5 V-tolerant I/O directly connected to ADC
		TC	Standard 5 V I/O
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

FCM32F072 pin definitions

Pin numbers			Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP48/UFQFPN48	UFQFPN32					Alternate functions	Additional functions
1	1		VBAT	S	-	-	Backup power supply	
2	2		PC13	I/O	TC	(1) (2)	-	WKUP2, RTC_TAMP1, RTC_TS, RTC_OUT
3	3		PC14 OSC32_IN	I/O	TC	(1) (2)	-	OSC32_IN
4	4		PC15 OSC32_OUT	I/O	TC	(1) (2)	-	OSC32_OUT
5	5	2	PF0 OSC_IN	I/O	FTf		CRS_ SYNC, I2C1_SDA	OSC_IN
6	6	3	PF1 OSC_OUT	I/O	FTf		I2C1_SCL	OSC_OUT
7	7	4	NRST	I/O	RST		Device reset input / internal reset output(active low)	
8	-		PC0	I/O	TTa		EVENTOUT, USART6_TX, USART7_TX	ADC_IN10

9	-		PC1	I/O	TTa		EVENTOUT, USART6_RX, USART7_RX	ADC_IN11
10	-		PC2	I/O	TTa		SPI2_MISO, I2S2_MCK, EVENTOUT, USART8_TX	ADC_IN12
11	-		PC3	I/O	TTa		SPI2_MOSI, I2S2_SD, EVENTOUT, USART8_RX	ADC_IN13
12	8		VSSA	S	-		Analog ground	
13	9	5	VDDA	S	-		Analog power supply	
14	10	6	PA0	I/O	TTa		USART2_CTS, TIM2_CH1_ETR, TSC_G1_IO1, USART4_TX COMP1_OUT	RTC_ TAMP2, WKUP1, ADC_IN0, COMP1_INM6
15	11	7	PA1	I/O	TTa		USART2_RTS, TIM2_CH2, TIM15_CH1N, TSC_G1_IO2, USART4_RX, EVENTOUT	ADC_IN1, COMP1_INP, *OPAMP1_VINP0*
16	12	8	PA2	I/O	TTa		USART2_TX, TIM2_CH3, TIM15_CH1, TSC_G1_IO3 COMP2_OUT	ADC_IN2, WKUP4, COMP2_INM6, *OPAMP1_VOUT*
17	13	9	PA3	I/O	TTa		USART2_RX,TIM2_CH4, TIM15_CH2, TSC_G1_IO4	ADC_IN3, COMP2_INP, *OPAMP1_VINM1*, *OPAMP1_VINP1*
18	-		VSS	S	-		Ground	
19	-		VDD	S	-		Digital power supply	
20	14	10	PA4	I/O	TTa		SPI1_NSS, I2S1_WS, TIM14_CH1, TSC_G2_IO1, USART2_CK, USART6_TX	COMP1_INM4, COMP2_INM4, ADC_IN4, DAC_OUT1
21	15	11	PA5	I/O	TTa		SPI1_SCK, I2S1_CK, CEC, TIM2_CH1_ETR, TSC_G2_IO2, USART6_RX	COMP1_INM5, COMP2_INM5, ADC_IN5, DAC_OUT2 *OPAMP1_VINP2*
22	16	12	PA6	I/O	TTa		SPI1_MISO, I2S1_MCK, TIM3_CH1, TIM1_BKIN, TIM16_CH1, COMP1_OUT, TSC_G2_IO3, EVENTOUT, USART3_CTS	ADC_IN6
23	17	13	PA7	I/O	TTa		SPI1_MOSI, I2S1_SD, TIM3_CH2, TIM14_CH1, TIM1_CH1N, TIM17_CH1, COMP2_OUT, TSC_G2_IO4, EVENTOUT	ADC_IN7 *OPAMP1_VINP3*
24	-		PC4	I/O	TTa		EVENTOUT, USART3_TX	ADC_IN14
25	-		PC5	I/O	TTa		TSC_G3_IO1, USART3_RX	ADC_IN15, WKUP5, *OPAMP1_VINM0*

26	18	14	PB0	/O	TTa		TIM3_CH3, TIM1_CH2N, TSC_G3_IO2, EVENTOUT, USART3_CK	ADC_IN8
27	19	15	PB1	I/O	TTa		TIM3_CH4, USART3_RTS, TIM14_CH1, TIM1_CH3N, TSC_G3_IO3	ADC_IN9
28	20	16	PB2	I/O	FT		TSC_G3_IO4	-
29	21		PB10	I/O	FTf		SPI2_SCK, I2S2_CK, I2C2_SCL, USART3_TX, CEC, TSC_SYNC, TIM2_CH3	-
30	22		PB11	I/O	FTf		USART3_RX, TIM2_CH4, EVENTOUT, TSC_G6_IO1, I2C2_SDA	-
31	23		VSS	S	-		Ground	
32	24	17	VDD	S	-		Digital power supply	
33	25		PB12	I/O	FT		TIM1_BKIN, TIM15_BKIN, SPI2_NSS, I2S2_WS, USART3_CK, TSC_G6_IO2, EVENTOUT ***CAN2_RX***	-
34	26		PB13	I/O	FTf		SPI2_SCK, I2S2_CK, I2C2_SCL, USART3_CTS, TIM1_CH1N, TSC_G6_IO3 ***CAN2_TX***	-
35	27		PB14	I/O	FTf		SPI2_MISO, I2S2_MCK, I2C2_SDA, USART3_RTS, TIM1_CH2N, TIM15_CH1, TSC_G6_IO4	-
36	28		PB15	I/O	FT		SPI2_MOSI, I2S2_SD, TIM1_CH3N, TIM15_CH1N, TIM15_CH2	WKUP7, RTC_REFIN
37	-		PC6	I/O	FT	(3)	TIM3_CH1, USART7_TX	-
38	-		PC7	I/O	FT	(3)	TIM3_CH2, USART7_RX	-
39	-		PC8	I/O	FT	(3)	TIM3_CH3, USART8_TX	-
40	-		PC9	I/O	FT	(3)	TIM3_CH4, USART8_RX	-
41	29	18	PA8	I/O	FT	(3)	USART1_CK, TIM1_CH1, EVENTOUT, MCO, CRS_SYNC ***I2S2EXT_SD***	-
42	30	19	PA9	I/O	FT	(3)	USART1_TX, TIM1_CH2, TIM15_BKIN, TSC_G4_IO1, I2C1_SCL	MCO
43	31	20	PA10	I/O	FT	(3)	USART1_RX, TIM1_CH3, TIM17_BKIN, TSC_G4_IO2, I2C1_SDA	-
44	32	21	PA11	I/O	FT	(3)	CAN_RX, USART1_CTS, TIM1_CH4, COMP1_OUT, TSC_G4_IO3, EVENTOUT, I2C2_SCL	USB_DM

45	33	22	PA12	I/O	FT	(3)	CAN_TX, USART1_RTS, TIM1_ETR, COMP2_OUT, TSC_G4_IO4, EVENTOUT, I2C2_SDA	USB_DP
46	34	23	PA13	I/O	FT	(3) (4)	IR_OUT, SWDIO	-
47	35		VSS	S	-		Ground	
48	36		VDDIO2	S	-		Digital power supply	
49	37	24	PA14	I/O	FT	(3) (4)	USART2_TX, SWCLK	-
50	38	25	PA15	I/O	FT	(3)	SPI1_NSS, I2S1_WS, USART2_RX, USART4_RTS, TIM2_CH1_ETR, EVENTOUT	-
51	-		PC10	I/O	FT	(3)	USART3_TX, USART4_TX	-
52	-		PC11	I/O	FT	(3)	USART3_RX, USART4_RX	-
53	-		PC12	I/O	FT	(3)	USART3_CK, USART4_CK, USART5_TX	-
54	-		PD2	I/O	FT	(3)	USART3_RTS, TIM3_ETR, USART5_RX	-
55	39	26	PB3	I/O	FT		SPI1_SCK, I2S1_CK, TIM2_CH2, TSC_G5_IO1, EVENTOUT, USART5_TX ***LLSI1_TXD***	-
56	40	27	PB4	I/O	FT		SPI1_MISO, I2S1_MCK, TIM17_BKIN, TIM3_CH1, TSC_G5_IO2, EVENTOUT, USART5_RX ***LLSI2_TXD***	-
57	41	28	PB5	I/O	FT		SPI1_MOSI, I2S1_SD, I2C1_SMBA, TIM16_BKIN, TIM3_CH2, USART5_CK_RTS ***CAN2_RX*** ***LLSI3_TXD***	WKUP6
58	42	29	PB6	I/O	FTf		I2C1_SCL, USART1_TX, TIM16_CH1N, TSC_G5_I03 ***CAN2_TX*** ***LLSI4_TXD***	
59	43	30	PB7	I/O	FTf		I2C1_SDA, USART1_RX, USART4_CTS, TIM17_CH1N, TSC_G5_IO4 ***LLSI5_TXD***	
60	44	31	PF11-BOOT0	I/O	FT		-	Boot memory selection
61	45	32	PB8	I/O	FTf		I2C1_SCL, CEC, TIM16_CH1, TSC_SYNC, CAN_RX ***LLSI6_TXD***	-

62	46		PB9	I/O	FTf		SPI2_NSS, I2S2_WS, I2C1_SDA, IR_OUT, TIM17_CH1, EVENTOUT, CAN_TX ***LLSI7_TXD***	-
63	47		VSS	S	-		Ground	
64	48	1	VDD	S	-		Digital power supply	

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
- The speed should not exceed 2 MHz with a maximum load of 30 pF.
- These GPIOs must not be used as current sources (e.g. to drive an LED).
2. After the first RTC domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers which are not reset by the system reset. For details on how to manage these GPIOs, refer to the RTC domain and RTC register descriptions in the reference manual.
3. Distinct VSSA pin is only available on 48-pin packages. On all other packages, the pin number corresponds to the VSS pin to which VSSA pad of the silicon die is connected.
4. PA8, PA9, PA10, PA11, PA12, PA13, PA14, PA15, PC6, PC7, PC8, PC9, PC10, PC11, PC12 and PD2 I/Os are supplied by VDDIO2.
5. Pin pair PA11/12 can be remapped in place of pin pair PA9/10 using SYSCFG_CFGR1 register.
6. After reset, these pins are configured as SWDIO and SWCLK alternate functions, and the internal pull-up on the SWDIO pin and the internal pull-down on the SWCLK pin are activated.

PA alternate functions selected

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	-	USART2_CTS	TIM2_CH1_ETR	TSC_G1_IO1	USART4_TX	-	-	COMP1_OUT
PA1	EVENTOUT	USART2_RTS	TIM2_CH2	TSC_G1_IO2	USART4_RX	TIM15_CH1N	-	-
PA2	TIM15_CH1	USART2_TX	TIM2_CH3	TSC_G1_IO3	-	-	-	COMP2_OUT
PA3	TIM15_CH2	USART2_RX	TIM2_CH4	TSC_G1_IO4	-	-	-	-
PA4	SPI1_NSS,I2S1_WS	USART2_CK	USB_NOE	TSC_G2_IO1	TIM14_CH1	USART6_TX	-	
PA5	SPI1_SCK,I2S1_CK	CEC	TIM2_CH1_ETR	TSC_G2_IO2	-	USART6_RX	-	-
PA6	SPI1_MISO,I2S1_MCK	TIM3_CH1	TIM1_BKIN	TSC_G2_IO3	-	TIM16_CH1	-	COMP1_OUT
PA7	SPI1_MOSI,I2S1_SD	TIM3_CH2	TIM1_CH1N	TSC_G2_IO4	TIM14_CH1	TIM17_CH1	-	COM2P_OUT
PA8	MCO	USART1_CK	TIM1_CH1	EVENTOUT	CRS_SYNC	-	*I2S2EXT_SD*	-
PA9	TIM15_BKIN	USART1_TX	TIM1_CH2	TSC_G4_IO1	I2C1_SCL	MCO	-	-
PA10	TIM17_BKIN	USART1_RX	TIM1_CH3	TSC_G4_IO2	I2C1_SDA	-	-	-
PA11	EVENTOUT	USART1_CTS	TIM1_CH4	TSC_G4_IO3	CAN1_RX	I2C2_SCL	-	COMP1_OUT
PA12	EVENTOUT	USART1_RTS	TIM1_ETR	TSC_G4_IO4	CAN1_TX	I2C2_SDA	-	COMP2_OUT
PA13	SWDIO	IR_OUT	USB_NOE	-	-	-	-	-
PA14	SWCLK	USART2_TX	-	-	-	-	-	-
PA15	SPI1_NSS,I2S1_WS	USART2_RX	TIM2_CH1_ETR	EVENTOUT	USART4_RTS	USB_NOE		-

PB alternate functions selected

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	EVENTOUT	TIM3_CH3	TIM1_CH2N	TSC_G3_IO2	USART3_CK	-	-	-
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	TSC_G3_IO3	USART3_RTS	-	-	-
PB2	-	-	-	TSC_G3_IO4	-	-	-	-
PB3	SPI1_SCK,I2S1_CK	EVENTOUT	TIM2_CH2	TSC_G5_IO1	USART5_TX	-	-	*LLSI1_TXD*
PB4	SPI1_MISO,I2S1_MCK	TIM3_CH1	EVENTOUT	TSC_G5_IO2	USART5_RX	TIM17_BKIN	-	*LLSI2_TXD*
PB5	SPI1_MOSI,I2S1_SD	TIM3_CH2	TIM16_BKIN	I2C1_SMBA	USART5_CK_RTS	-	*CAN2_RX*	*LLSI3_TXD*
PB6	USART1_TX	I2C1_SCL	TIM16_CH1N	TSC_G5_IO3	-	-	*CAN2_TX*	*LLSI4_TXD*
PB7	USART1_RX	I2C1_SDA	TIM17_CH1N	TSC_G5_IO4	USART4_CTS	-	-	*LLSI5_TXD*
PB8	CEC	I2C1_SCL	TIM16_CH1	TSC_SYNC	CAN1_RX	-	-	*LLSI6_TXD*
PB9	IR_OUT	I2C1_SDA	TIM17_CH1	EVENTOUT	CAN1_TX	SPI2_NSS	-	*LLSI7_TXD*
PB10	CEC	I2C2_SCL	TIM2_CH3	TSC_SYNC	USART3_TX	SPI2_SCK	-	-
PB11	EVENTOUT	I2C2_SDA	TIM2_CH4	TSC_G6_IO1	USART3_RX	-	-	-
PB12	SPI2_NSS,I2S2_WS	EVENTOUT	TIM1_BKIN	TSC_G6_IO2	USART3_CK	TIM15_BKIN	*CAN2_RX*	-
PB13	SPI2_SCK,I2S2_CK	-	TIM1_CH1N	TSC_G6_IO3	USART3_CTS	I2C2_SCL	*CAN2_TX*	-
PB14	SPI2_MISO,I2S2_MCK	TIM15_CH1	TIM1_CH2N	GSC_G6_IO4	USART3_RTS	I2C2_SDA	-	-
PB15	SPI2_MOSI,I2S2_SD	TIM15_CH2	TIM1_CH3N	TIM15_CH1N	-	-	-	-

PC alternate functions selected

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC0	EVENTOUT	USART7_TX	USART6_TX				-	-
PC1	EVENTOUT	USART7_RX	USART6_RX				-	-
PC2	EVENTOUT	SPI2_MISO,I2S2_MCK	USART8_TX				-	-
PC3	EVENTOUT	SPI2_MOSI,I2S2_SD	USART8_RX				-	-
PC4	EVENTOUT	USART3_TX					-	-
PC5	TSC_G3_IO1	USART3_RX					-	-
PC6	TIM3_CH1	USART7_TX					-	-
PC7	TIM3_CH2	USART7_RX					-	-
PC8	TIM3_CH3	USART8_TX					-	-
PC9	TIM3_CH4	USART8_RX					-	-
PC10	USART4_TX	USART3_TX					-	-
PC11	USART4_RX	USART3_RX					-	-
PC12	USART4_CK	USART3_CK	USART5_TX				-	-
PC13	-						-	-
PC14	-						-	-
PC15	-						-	-

PD alternate functions selected

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PD2	TIM3_ETR	USART3_RTS	USART5_RX				-	-

PF alternate functions selected

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PF0	CRS_SYNC	I2C1_SDA	-	-	-	-	-	-
PF1	-	I2C1_SCL	-	-	-	-	-	-
PF2	EVENTOUT	USART7_TX	USART7_CK_RTS					
PF4	EVENTOUT							
PF5	EVENTOUT							
PF6		I2C2_SCL						
PF7		I2C2_SDA						
PF9	TIM15_CH1	USART6_TX						
PF10	TIM15_CH2	USART6_RX						
PF11								

5 Memory mapping

To the difference of FCM32F072xB/xC, the code memory spaces end at 0x0801FFFF and 0x0803FFFF, respectively.

FCM32F072 peripheral register boundary addresses

Bus	Boundary address	Size	Peripheral
-	0x4800 2000 – 0x4FFF FFFF	~127 MB	-
AHB2	0x4800 1C00 – 0x4800 1FFF	1KB	
	0x4800 1800 – 0x4800 1BFF	1KB	
	0x4800 1400 – 0x4800 17FF	1KB	GPIOF
	0x4800 1000 – 0x4800 13FF	1KB	-
	0x4800 0C00 – 0x4800 0FFF	1KB	GPIOD
	0x4800 0800 – 0x4800 0BFF	1KB	GPIOC
	0x4800 0400 – 0x4800 07FF	1KB	GPIOB
	0x4800 0000 – 0x4800 03FF	1KB	GPIOA
	0x4002 4400 – 0x47FF FFFF	~128MB	-
AHB1	0x4002 4000 – 0x4002 43FF	1KB	TSC
	0x4002 3400 – 0x4002 3FFF	3KB	-
	0x4002 3000 – 0x4002 33FF	1KB	CRC/HAU
	0x4002 2400 – 0x4002 2FFF	3KB	-
	0x4002 2000 – 0x4002 23FF	1KB	Flash memory interface
	0x4002 1400 – 0x4002 1FFF	3KB	-
	0x4002 1000 – 0x4002 13FF	1KB	RCC
	0x4002 0800 – 0x4002 0FFF	2KB	-
	0x4002 0400 – 0x4002 07FF	1KB	DMA2
	0x4002 0000 – 0x4002 03FF	1KB	DMA
APB2	0x4001 8000 – 0x4001 FFFF	32KB	-
	0x4001 7C00 – 0x4001 7FFF	1KB	
	0x4001 7800 – 0x4001 7BFF	1KB	
	0x4001 7400 – 0x4001 77FF	1KB	***LLSI***
	0x4001 7000 – 0x4001 73FF	1KB	-
	0x4001 6C00 – 0x4001 6FFF	1KB	-
	0x4001 6800 – 0x4001 6BFF	1KB	
	0x4001 6400 – 0x6001 67FF	1KB	-
	0x4001 6000 – 0x4001 63FF	1KB	
	0x4001 5C00 – 0x4001 5FFF	1KB	-
	0x4001 5800 – 0x4001 5BFF	1KB	DBGMCU
	0x4001 4C00 – 0x4001 57FF	3KB	-
	0x4001 4800 – 0x4001 4BFF	1KB	TIM17
	0x4001 4400 – 0x4001 47FF	1KB	TIM16
	0x4001 4000 – 0x4001 43FF	1KB	TIM15
	0x4001 3C00 – 0x4001 3FFF	1KB	-
	0x4001 3800 – 0x4001 3BFF	1KB	USART1
	0x4001 3400 – 0x4001 37FF	1KB	-
	0x4001 3000 – 0x4001 33FF	1KB	SPI1/I2S1
	0x4001 2C00 – 0x4001 2FFF	1KB	TIM1
	0x4001 2800 – 0x4001 2BFF	1KB	-

	0x4001 2400 – 0x4001 27FF	1KB	ADC
	0x4001 2000 – 0x4001 23FF	1KB	-
	0x4001 1C00 – 0x4001 1FFF	1KB	USART8
	0x4001 1800 – 0x4001 1BFF	1KB	USART7
	0x4001 1400 – 0x4001 17FF	1KB	USART6
	0x4001 0800 – 0x4001 13FF	3KB	-
	0x4001 0400 – 0x4001 07FF	1KB	EXTI
	0x4001 0000 – 0x4001 03FF	1KB	SYSCFG/COMP/AMP
APB1	0x4000 C000 – 0x4000 FFFF	21KB	-
	0x4000 A800 – 0x4000 ABFF	1KB	-
	0x4000 A400 – 0x4000 A7FF	1KB	-
	0x4000 7C00 – 0x4000 A3FF	10KB	-
	0x4000 7800 – 0x4000 7BFF	1KB	CEC
	0x4000 7400 – 0x4000 77FF	1KB	DAC
	0x4000 7000 – 0x4000 73FF	1KB	PWR
	0x4000 6C00 – 0x4000 6FFF	1KB	CRS
	0x4000 6800 – 0x4000 6BFF	1KB	bxCAN2*/exCAN2*
	0x4000 6400 – 0x4000 67FF	1KB	bxCAN1*/exCAN1/USBHD RAM 2nd 1KB*
	0x4000 6000 – 0x4000 63FF	1KB	USBHD RAM 1st 1KB
	0x4000 5C00 – 0x4000 5FFF	1KB	USBHD
	0x4000 5800 – 0x4000 5BFF	1KB	I2C2
	0x4000 5400 – 0x4000 57FF	1KB	I2C1
	0x4000 5000 – 0x4000 53FF	1KB	USART5
	0x4000 4C00 – 0x4000 4FFF	1KB	USART4
	0x4000 4800 – 0x4000 53FF	1KB	USART3
	0x4000 4400 – 0x4000 47FF	1KB	USART2
	0x4000 4000 – 0x4000 43FF	1KB	-
	0x4000 3C00 – 0x4000 3FFF	1KB	-
	0x4000 3800 – 0x4000 3BFF	1KB	SPI2/I2S2
	0x4000 3400 – 0x4000 37FF	1KB	*I2S2EXT*
	0x4000 3000 – 0x4000 33FF	1KB	IWDG
	0x4000 2C00 – 0x4000 2FFF	1KB	WWDG
	0x4000 2800 – 0x4000 2BFF	1KB	RTC
	0x4000 2400 – 0x4000 27FF	1KB	-
	0x4000 2000 – 0x4000 23FF	1KB	TIM14
	0x4000 1800 – 0x4000 1FFF	2KB	-
	0x4000 1400 – 0x4000 17FF	1KB	TIM7
	0x4000 1000 – 0x4000 13FF	1KB	TIM6
	0x4000 0800 – 0x4000 0FFF	2KB	-
	0x4000 0400 – 0x4000 07FF	1KB	TIM3
	0x4000 0000 – 0x4000 03FF	1KB	TIM2

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25C and T_A = $T_A$max (given by the selected temperature range).

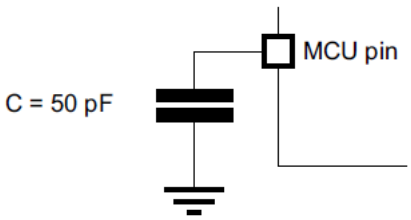
6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A=25C, VDD=VDDA=3.3V. They are given only as design guidelines and are not tested.

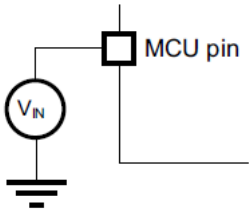
6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor



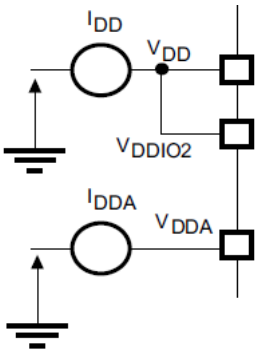
6.1.5 Pin input voltage



6.1.6 Power supply scheme

Each power supply pair (VDD/VSS, VDDA/VSSA etc.) must be decoupled with filtering ceramic capacitors. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

6.1.7 Current consumption measurement



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}-V_{SS}	External main supply voltage	-0.3	5.8	V
V_{DDIO2}-V_{SS}	External I/O supply voltage	-0.3	5.8	V
V_{DDA}-V_{SS}	External analog supply voltage	-0.3	5.8	V
V_{DD}-V_{DDA}	Allowed voltage difference for V_{DD}>V_{DDA}	-	0.3	V
V_{BAT}-V_{SS}	External backup supply voltage	-0.3	5.8	V
V_{IN}	Input voltage on FT and FTf pins	V_{SS}-0.3	V_{DDIOx}+0.3	V
	Input voltage on TTa pins	V_{SS}-0.3	5.8	V
	Input voltage on any other pins	V_{SS}-0.3	5.8	V

$\lvert\triangle V_{DDx}\rvert$	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{SSx}-V_{SS}\rvert$	Variations between all the different ground pins	-	50	mV
V_{ESD}(HBM)	Electrostatic discharge voltage		3000	V

6.3 Operating conditions

6.3.1 General operating conditions

General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	72	MHz
f_{PCLK}	Internal APB clock frequency	-	0	72	MHz
V_{DD}	Standard operating voltage	-	1.8	5.5	V
V_{DDIO2}	I/O supply voltage		1.65	5.5	V
V_{DDA}	Analog operating voltage		V_{DD}	5.5	V
V_{BAT}	Backup operating voltage		2.1	5.5	V
V_{IN}	I/O input voltage	TC and RST I/O	-0.3	V_{DDIOx}+0.3	V
		TTa I/O	-0.3	V_{DDA}+0.3	
		FT and FTf I/O	-0.3	5.5	
P_D	Power dissipation at TA=85C	LQFP48	-	350	mW
		UFQFPN48	-	600	
		LQFP32		350	
		UFQFPN32		500	
		UFQFPN28		170	
		TSSOP20		250	
TA	Ambient temperature for the suffix 6 version	Maximum power dissipation	-20	85	C
		Low power dissipation	-20	105	
	Ambient temperature for the suffix 7 version	Maximum power dissipation	-40	105	C
		Low power dissipation	-40	125	
TJ	Junction temperature range	Suffix 6 version	-40	105	C
		Suffix 7 version	-40	125	

6.3.2 Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	VDD rise time rate	-	0	∞	us/V
	VDD fall time rate		20	∞	
t_{VDDA}	VDDA rise time rate	-	0	∞	
	VDDA fall time rate		20	∞	

6.3.3 Embedded reset and power control block characteristics

Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{POR/PDR}$	Power on/down reset threshold	Falling edge	1.51	1.58	1.65	V
		Rising edge	1.54	1.62	1.70	
$V_{PDRhyst}$	PDR hysteresis	-	-	40	-	mV
$t_{RSTTEMPO}$	Reset temporization	-	1.5	2.5	4.5	ms

Programmable voltage detector characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD0}	PVD threshold 0	Falling edge	1.59	1.67	1.75	V
		Rising edge	1.75	1.83	1.91	
V_{PVD1}	PVD threshold 1	Falling edge	1.75	1.83	1.91	
		Rising edge	1.90	1.98	2.06	
V_{PVD2}	PVD threshold 2	Falling edge	1.90	1.98	2.06	
		Rising edge	2.06	2.14	2.22	
V_{PVD3}	PVD threshold 3	Falling edge	2.06	2.14	2.22	
		Rising edge	2.21	2.29	2.37	
V_{PVD4}	PVD threshold 4	Falling edge	2.21	2.29	2.37	
		Rising edge	2.35	2.43	2.51	
V_{PVD5}	PVD threshold 5	Falling edge	2.35	2.43	2.51	
		Rising edge	2.49	2.57	2.65	
V_{PVD6}	PVD threshold 6	Falling edge	2.49	2.57	2.65	
		Rising edge	2.64	2.72	2.80	
V_{PVD7}	PVD threshold 7	Falling edge	2.64	2.72	2.80	
		Rising edge	2.80	2.88	2.96	
$V_{PVDhyst}$	PVD hysteresis	-	-	160	-	mV
$I_{DD(PVD)}$	PVD current consumption	-		0.15		uA

6.3.4 Embedded reference voltage

Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	-40C<TA<+105	1.22	1.23	1.24	V
t_{START}	ADC_IN17 buffer startup time	-		-	10	us
$t_{S_vrefint}$	ADC sampling time when reading the internal reference voltage	-	8	-	-	us
$\triangle V_{REFINNT}$	Internal reference voltage spread over the temperature range	V_{DDA}=3V	-	-	10	mV
T_{Coeff}	Temperature coefficient	-	-	-	100	ppm/C

6.3.5 Supply current characteristics

Typical current consumption (VDD+VDDA @ 3.6V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD}+I_{DDA}$	Run from Flash memory	All peripherals enabled, HSI 8MHz		4.5		mA
		All peripherals enabled, HSI48		25.4		
		All peripherals enabled, HSI + PLL 72MHz		35.2		
	Stop mode	Regulator in low-power mode, all oscillators OFF		18.3		uA
	Standby mode	Regulator in low-power mode, all oscillators OFF		7.6		uA

6.3.6 Wakeup time from low-power mode

Low-power mode wakeup timings

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{WUSTOP}	Wakeup from stop mode	Regulator in run mode	-	11		us
t_{START}		Regulator in low power mode		11		
$t_{WUSTANNDBY}$	Wakeup from standby mode	-	-	50	-	
$t_{WUSLEEP}$	Wakeup from sleep mode	-	4 SYSCLK cycles			

6.3.7 External clock source characteristics

High-speed external user clock characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{HSE_EXT}	User external clock source frequency	-	8	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage	$0.7*V_{DDIOx}$	-	V_{DDIOx}	V
V_{HSEL}	OSC_IN input pin low level voltage	VSS	-	$0.3*V_{DDIOx}$	
$t_{W(HSEH)}$ $t_{W(HSEL)}$	OSC_IN high or low time	15	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time	-	-	20	

Low-speed external user clock characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSE_EXT}	User external clock source frequency	-	32.768	1000	KHz
V_{LSEH}	OSC32_IN input pin high level voltage	$0.7*V_{DDIOx}$	-	V_{DDIOx}	V
V_{LSEL}	OSC32_IN input pin low level voltage	VSS	-	$0.3*V_{DDIOx}$	
$t_{W(LSEH)}$ $t_{W(LSEL)}$	OSC32_IN high or low time	450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time	-	-	50	

HSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	20	MHz
RF	Feedback resistor	-	-	200	-	KΩ
I_{DD}	HSE current consumption	VDD=3.3V, Rm=45Ω, CL=10pF@8MHz		0.57		mA
g_m	Oscillator transconductance	Startup	10	-	-	mA/V
$t_{SU(HSE)}$	Startup time	VDD is stabilized	-	2	-	ms

LSE oscillator characteristics (f_{LSE}=32.768KHz)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	LSE current consumption	low drive capability		360		nA
		medium-low drive capability		450		
		medium-high drive capability		540		
		high drive capability		700		
g_m	Oscillator transconductance	low drive capability	5	-	-	uA/V
		medium-low drive capability	8			
		medium-high drive capability	15			
		high drive capability	25			
$t_{SU(LSE)}$	Startup time	V_{DDIOx} is stabilized	-	2	-	s

6.3.8 Internal clock source characteristics

HSI48 oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI48}	Frequency	-		48		MHz
TRIM	HSI48 user-trimming step	-		0.15		%
DuCy	Duty cycle	-	45	-	55	%
ACC_{HSI48}	Accuracy of the HSI48 oscillator(factory calibrated)	TA=-40 to 105 @SS	-1.84		2.00	%
		TA=-40 to 105@TT	-1.58		1.76	
		TA=-40 to 105@FF	-1.24		1.72	
$t_{SU(HSI48)}$	HSI48 oscillator startup time	-			6	us
$I_{DDA(HSI48)}$	HSI48 oscillator power consumption	-		643	801	uA

LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	31.9	40	55.5	KHz
$t_{SU(LSI)}$	LSI oscillator startup time	-			100	us
$I_{DDA(LSI)}$	LSI oscillator power consumption	-		400		nA

6.3.9 PLL characteristics

PLL characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	1	8	24	MHz
t_{PLL_OUT}	PLL multiplier output clock	16		96	MHz

t_{LOCK}	PLL lock time	30		100	us
$I_{DDA(PLL)}$	PLL power consumption			350	uA
$Jitter_{PLL}$	Cycle-to-cycle jitter			300	ps

6.3.10 Memory characteristics

Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PROG}	16-bit programming time	TA=-40 to +125		20		us
t_{ERASE}	Page(1KB) erase time			18		ms
t_{ME}	Mass erase time			30		ms
I_{DD}	Supply current	Write mode			3.5	mA
		Erase mode			2	mA
N_{END}	Endurance	TA=-40 to +125	20			kcycle
t_{RET}	Data retention	TA=25C	100			Year

6.3.11 EMC characteristics

EMC characteristics

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	VDD=3.3V, LQFP48, TA=25C, f_{HCLK}=48 MHz, conforming to IEC 61000-4-2	3B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100pF on V_{DD} and V_{SS} pins to induce a functional disturbance	VDD=3.3V, LQFP48, TA=25C, f_{HCLK}=48 MHz, conforming to IEC 61000-4-4	4B

EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs.[f_{HSE}/f_{HCLK}] 8/48 MHz	Unit
SEMI	Peak level	VDD=3.6V, TA=25C, LQFP48 package compliant with IEC 61967-2	0.1 to 30MHz		dBuV
			30 to 130MHz		
			130 MHz to 1GHz		
			EMI level		-

6.3.12 Electrical sensitivity characteristics

ESD absolute maximum ratings

Symbol	Parameter	Conditions	Packages	Class	Maxi value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	TA=+25C, conforming to JESD22-A114	All	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	TA=+25C, conforming to AEC-Q100-011	All	C6	750	V

6.3.13 I/O current injection characteristics

I/O current injection susceptibility

Symbol	Parameter	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current	-5	+5	mA

6.3.14 I/O port characteristics

I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	TC and TTa I/O			$0.3*V_{DDIOx}$	V
		FT and FTf I/O			$0.475*V_{DDIOx}-0.2$	
		All I/Os			$0.3*V_{DDIOx}$	
V_{IH}	High level input voltage	TC and TTa I/O	$0.445*V_{DDIOx}+0.4$			V
		FT and FTf I/O	$0.5*V_{DDIOx}+0.2$			
		All I/Os	$0.7*V_{DDIOx}$			
V_{hys}	Schmitt trigger hysteresis	TC and TTa I/O		200		mV
		FT and FTf I/O		100		
I_{lkg}	Input leakage current	TC,FT and FTf I/O TTa in digital mode $V_{SS}<=V_{IN}<=V_{DDIOx}$			±0.1	uA
		TTa in digital mode $V_{DDIOx}<=V_{IN}<=V_{DDA}$			1	
		TTa in analog mode $V_{SS}<=V_{IN}<=V_{DDA}$			±0.2	
		FT and FTf I/O $V_{DDIOx}<=V_{IN}<=5V$			10	
R_{PU}	Weak pull-up resistor	$V_{IN}=V_{SS}$		40		KΩ
R_{PD}	Weak pull-down resistor	$V_{IN}=-V_{DDIOX}$		40		KΩ
C_{IO}	I/O pin capacitance			5		pF

Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage for an I/O pin	CMOS port $\|I_{IO}\|$ = 8mA $V_{DDIOx}>=2.7V$	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		$V_{DDIOx}-0.4$	-	
V_{OL}	Output low level voltage for an I/O pin	TTL port $\|I_{IO}\|$ = 8mA $V_{DDIOx}>=2.7V$	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		2.4	-	
V_{OL}	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 20mA $V_{DDIOx}>=2.7V$	-	1.3	V
V_{OH}	Output high level voltage for an I/O pin		$V_{DDIOx}-1.3$	-	
V_{OL}	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 6mA $V_{DDIOx}>=2.7V$	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		$V_{DDIOx}-0.4$	-	
V_{OL}	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 4mA	-	0.4	V

V_{OH}	Output high level voltage for an I/O pin	V_{DDIOx}>= 2.7V	V_{DDIOx}-0.4	-	
V_{OLFm+}	Output low level voltage for an FTf I/O pin in FM+ mode	$\|I_{IO}\|$ = 20mA V_{DDIOx}>= 2.7V	-	0.4	V
		$\|I_{IO}\|$ = 10mA	-	0.4	

I/O AC characteristics

OSPEEDRy [1:0]	Symbol	Parameter	Conditions	Min	Max	Unit
x0	$f_{max(IO)out}$	Maximum frequency	C_L=50pF, V_{DDIOx}>=2V	-	2	MHz
	$t_{f(IO)out}$	Output fall time		-	38	ns
	$t_{r(IO)out}$	Output rise time		-	39	
01	$f_{max(IO)out}$	Maximum frequency	C_L=50pF, V_{DDIOx}>=2V	-	10	MHz
	$t_{f(IO)out}$	Output fall time		-	25	ns
	$t_{r(IO)out}$	Output rise time		-	25	
11	$f_{max(IO)out}$	Maximum frequency	C_L=30pF, V_{DDIOx}>=2.7V	-	50	MHz
			C_L=50pF, V_{DDIOx}>=2.7V	-	30	
			C_L=50pF, 2V<=V_{DDIOx}<2.7V	-	20	
	$t_{f(IO)out}$	Output fall time	C_L=30pF, V_{DDIOx}>=2.7V	-	6.5	ns
			C_L=50pF, V_{DDIOx}>=2.7V	-	9	
			C_L=50pF, 2V<=V_{DDIOx}<2.7V	-	15.5	
	$t_{r(IO)out}$	Output rise time	C_L=30pF, V_{DDIOx}>=2.7V	-	6.6	
			C_L=50pF, V_{DDIOx}>=2.7V	-	8.6	
			C_L=50pF, 2V<=V_{DDIOx}<2.7V	-	39	
Fm+ configuration	$f_{max(IO)out}$	Maximum frequency	C_L=50pF, V_{DDIOx}>=2V	-	2	MHz
	$t_{f(IO)out}$	Output fall time		-	15.5	ns
	$t_{r(IO)out}$	Output rise time		-	39	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	-	ns

6.3.15 NRST pin characteristics

NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	0.3*VDD	V
$V_{IH(NRST)}$	NRST input high level voltage	-	0.445*VDD+0.4	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up resistor	V_{IN}=V_{SS}	-	40	-	KΩ
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	2.7<VDD<3.6	300	-	-	ns
		2.0<VDD<3.6	500	-	-	

6.3.16 ADC characteristics

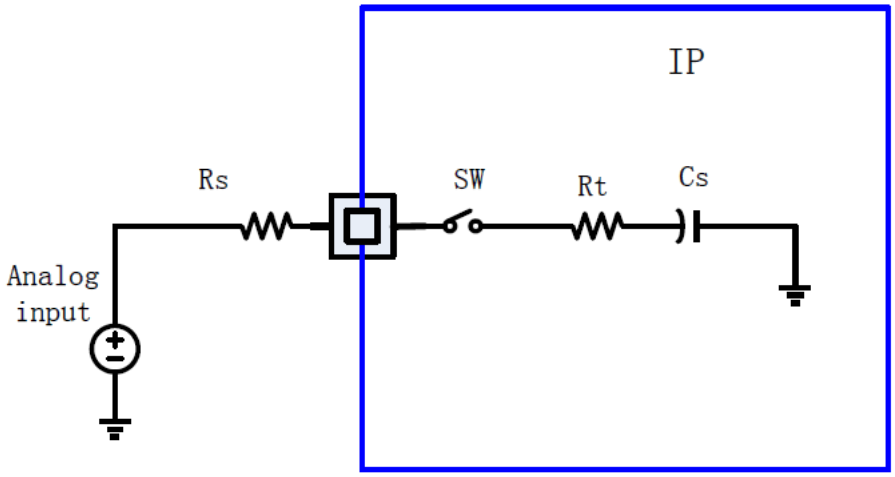
ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.8	3.3	5.5	V
$I_{DD(ADC)}$	Current consumption of the ADC	V_{DDA}=3.3V	-	1.1	-	mA
f_{ADC}	ADC clock frequency	-	-	-	16	MHz
f_S	Sampling rate	12-bit resolution	0.03	-	1	MHz
f_{TRIG}	External trigger frequency	12-bit resolution	-	-	18	$1/f_{ADC}$
V_{AIN}	Conversion voltage range		0		V_{DDA}	V
R_t	Input resistor during sampling	V_{DDA}=3V		0.5		kΩ
C_s	Internal sample and hold capacitor			26	30	pF
t_S	Sampling time	f_{ADC}=16MHz	4	-	-	$1/f_{ADC}$
t_{STAB}	Stabilization time		32	-	-	$1/f_{ADC}$
t_{CONV}	Total conversion time	12-bit resolution		12		$1/f_{ADC}$

ADC accuracy

Symbol	Parameter	Conditions	Typ	Max	Unit
ET	Total unadjusted error	f_{PCLK}=48MHz, f_{ADC}=16MHz,RAIN<10kΩ V_{DDA}=3V to 3.6V TA=25C	±1.5	-	LSB
EO	Offset error		±1.5	±3.0	
EG	Gain error		±2	±5	
ED	Differential linearity error		±0.6	±1.5	
EL	Integral linearity error		±1.5	±3.0	

Analog Input Equivalent Circuit



$$Rs = \frac{Tsamp}{10 * Cs} - Rt$$

R_{AIN} max for f_{ADC} = 16 MHz

T_s(cycles)	t_s(us)	RAIN max (kΩ)
4	0.35	0.33
7.5	0.47	1.1
13.5	0.84	2.3
28.5	1.78	5.4
41.5	2.59	8.1
55.5	3.47	11.1
71.5	4.47	14.4
239.5	14.97	49.4

6.3.17 DAC characteristics

DAC characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Commnets
V_{DDA}	Analog suplly voltage for DAC ON	1.8	-	5.5	V	
R_{LOAD}	Resistive load with buffer ON	5	-	-	kΩ	
R_O	Impedance output with buffer OFF	-	-	12	kΩ	
C_{LOAD}	Capacitive load	-	-	50	pF	
DAC_OUT min	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	
DAC_OUT max	Higher DAC_OUT voltage with buffer ON	-	-	V_{DDA}-0.2	V	
DAC_OUT min	Lower DAC_OUT voltage with buffer OFF	-	0.5	-	mV	
DAC_OUT max	Higher DAC_OUT voltage with buffer OFF	-	-	V_{DDA}-1LSB	V	
I_{DDA}	DAC DC current consumption in quiescent mode	-	-	362	uA	With no load, middle code (0x800) on the input
				506		With no load, middle code (0xF1C) on the input
DNL	Differential non linearity (Difference between two consecutive code-1LSB)	-	-	+/-0.5	LSB	Given for the DAC in 10-bit configuration
				+/-2		Given for the DAC in 12-bit configuration
INL	Integral non linearity (difference between measured value at Code I and the value at Code I on a line drawn between Code 0 and last Code 1023)	-	-	+/-1	LSB	Given for the DAC in 10-bit configuration
		-	-	+/-4		Given for the DAC in 12-bit configuration
Offset	Offset error (difference between measured value at Code 0x800 and the ideal value = V_{DDA}/2	-	-	+/-10	mV	
		-	-	+/-3	LSB	Given for the DAC in 10-bit configuration
		-	-	+/-12		Given for the DAC in 12-bit configuration
Gain error	Gain error	-	-	+/-0.2	%	Given for the DAC in 12-bit configuration
$t_{SETTLING}$	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value +/-1LSB	-	3	4	us	C_{LOAD} <=50 pF, R_{LOAD} >= 50 kΩ
Update rate	Max frequency for a correct DAC_OUT change when small variation in the input code (from code I to i+1LSB)	-	-	1	MS/s	C_{LOAD} <=50 pF, R_{LOAD} >= 50 kΩ

t_{WAKEUP}	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	6.5	10	us	C_{LOAD} <=50 pF, R_{LOAD} >= 50 kΩ input code between lowest and highest possible ones
PSRR+	Power supply rejection ratio (to V_{DDA}) (static DC measurement)	-			dB	No R_{LOAD}, C_{LOAD} = 50pF

6.3.18 COMP characteristics

Comparator characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog suplly voltage			V_{DD}	-	5.5	V
V_{IN}	Comparator input voltage range			0	-	V_{DDA}	V
V_{SC}	V_{REFINT} scaler offset voltage			-	+/-5	+/-10	mV
ts_sc	V_{REFINT} scaler startup time from power down	First V_{REFINT} scaler activation after device power on		-	-	1000	ms
		Next activations		-	-	0.2	ms
t_{START}	Comparator startup time	Startup time to reach propagation delay specification		-	-	60	us
t_D	Propagation delay for 200mV step with 100mV overdrive	Ultra-low power mode					us
		Low power mode					
		Medium power mode					
		High speed mode	V_{DDA} >= 2.7V				ns
			V_{DDA}<2.7V				
	Propagation delay for full range step with 100mV overdrive	Ultra-low power mode		-	0.300	-	us
		Low power mode			0.160	-	
		Medium power mode			0.078	-	
		High speed mode	V_{DDA} >= 2.7V		18		ns
V_{offset}	Comparator offset error			-	+/-5	-	mV
dV_{offset}/dT	Offset error temperature coefficient			-	-	-	uV/C
I_{DD}	Comparator current consumption	Ultra-low power mode		-	1.3	-	uA
		Low power mode		-	3	-	
		Medium power mode		-	12	-	
		High speed mode		-	80	-	
V_{hyst}	Comparator hysteresis	No hysteresis	-	-	0	-	mV
		Low hysteresis	High speed mode		8		
			All other power modes		8		
		Medium hysteresis	High speed mode		16		
			All other power modes		16		

		High hysteresis	High speed mode		30		
			All other power modes		32		

6.3.19 Temperature sensor characteristics

TS characteristics

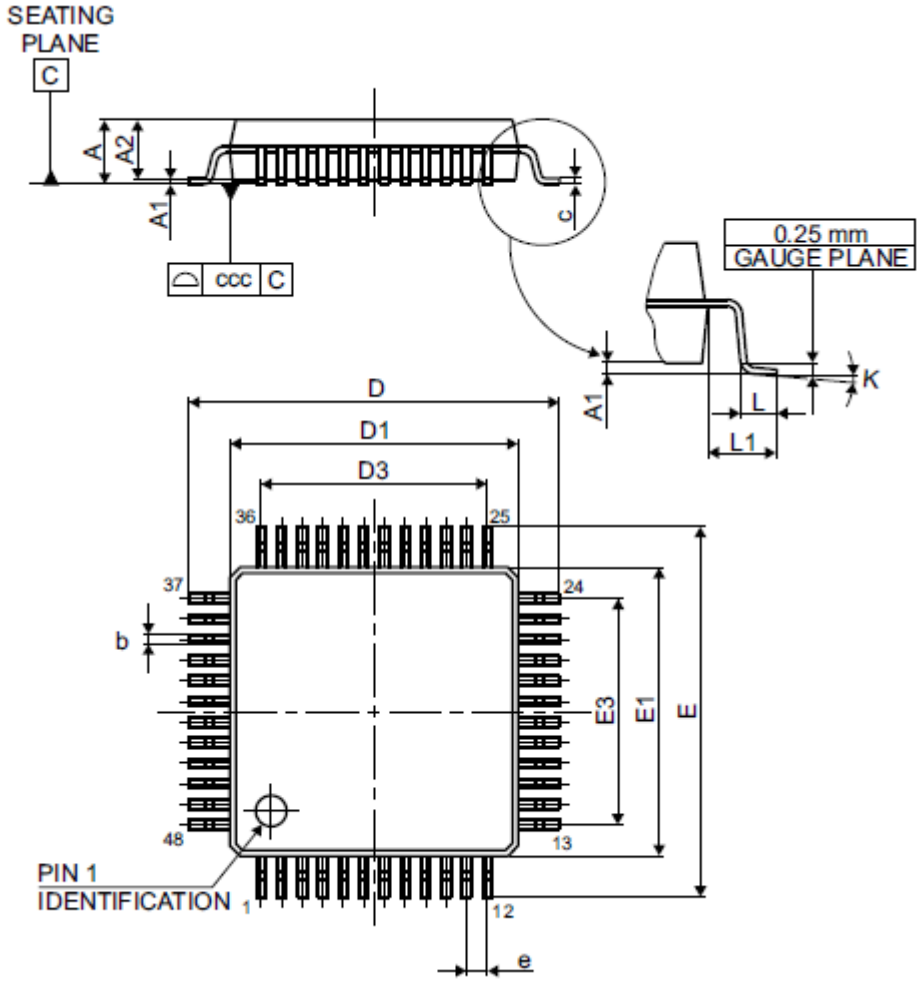
Symbol	Parameter	Min	Typ	Max	Unit
T_L	V_{SENSE} linearity with temperature	-	±1	±2	C
Avg_Slope	Average slope	4.2	4.28	4.36	mV/C
V30	Voltage at 30C	1.423	1.425	1.43	V
tSTART	ADC_IN16 buffer startup time	1	-	5	us
t_{S_temp}	ADC sampling time when reading the temperature	4	-	-	us

7 Package information

7.1 LQFP48 package information

LQFP48 is a 48-pin, 7 x 7 mm low-profile quad flat package.

LQFP48 package outline



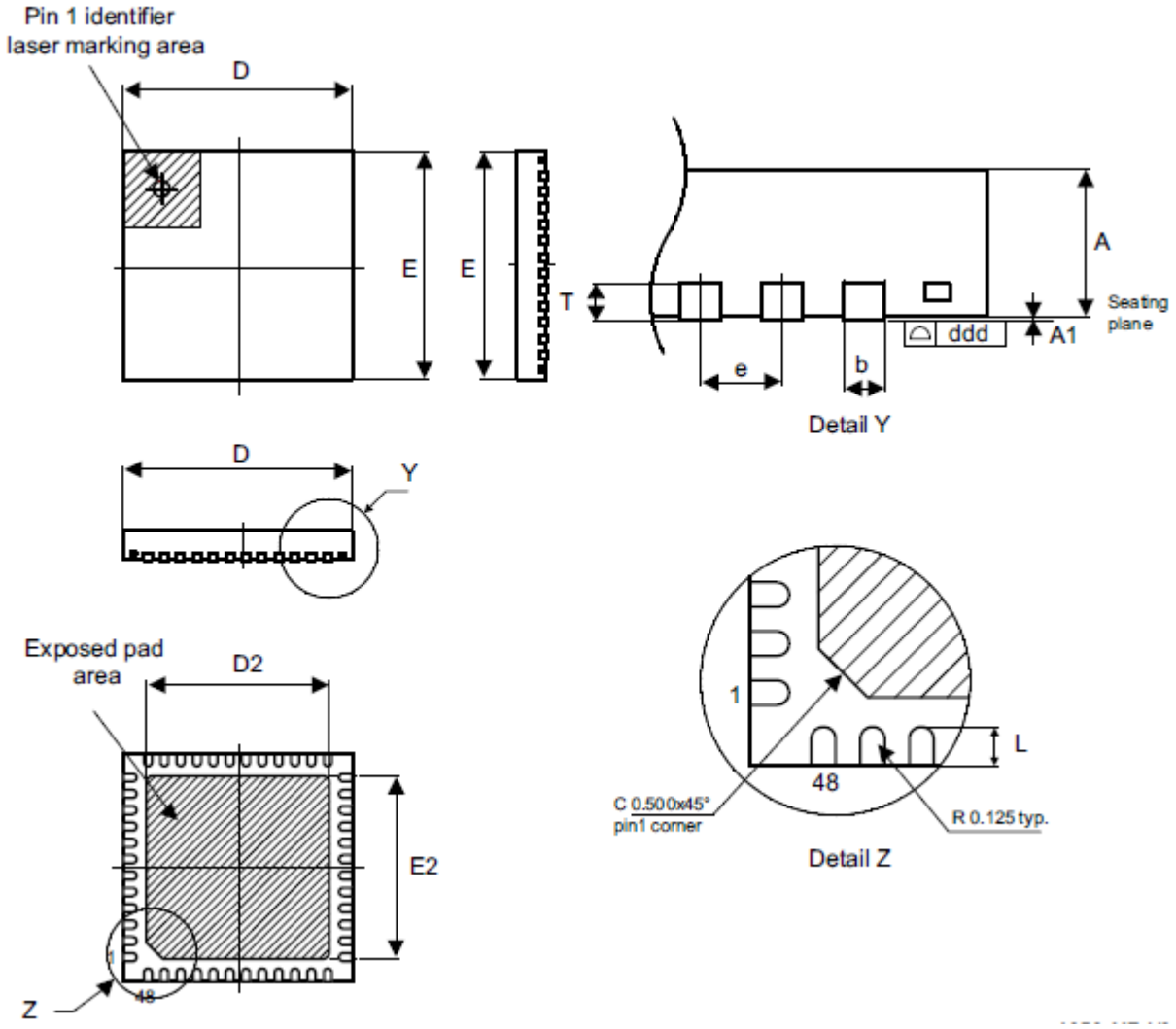
LQFP48 package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

7.2 UFQFPN48 package information

UFQFPN48 is a 48-lead, 7 x 7 mm, 0.5 mm pitch, fine-pitch quad flat package.

UFQFPN48 package outline



UFQFPN48 package mechanical data

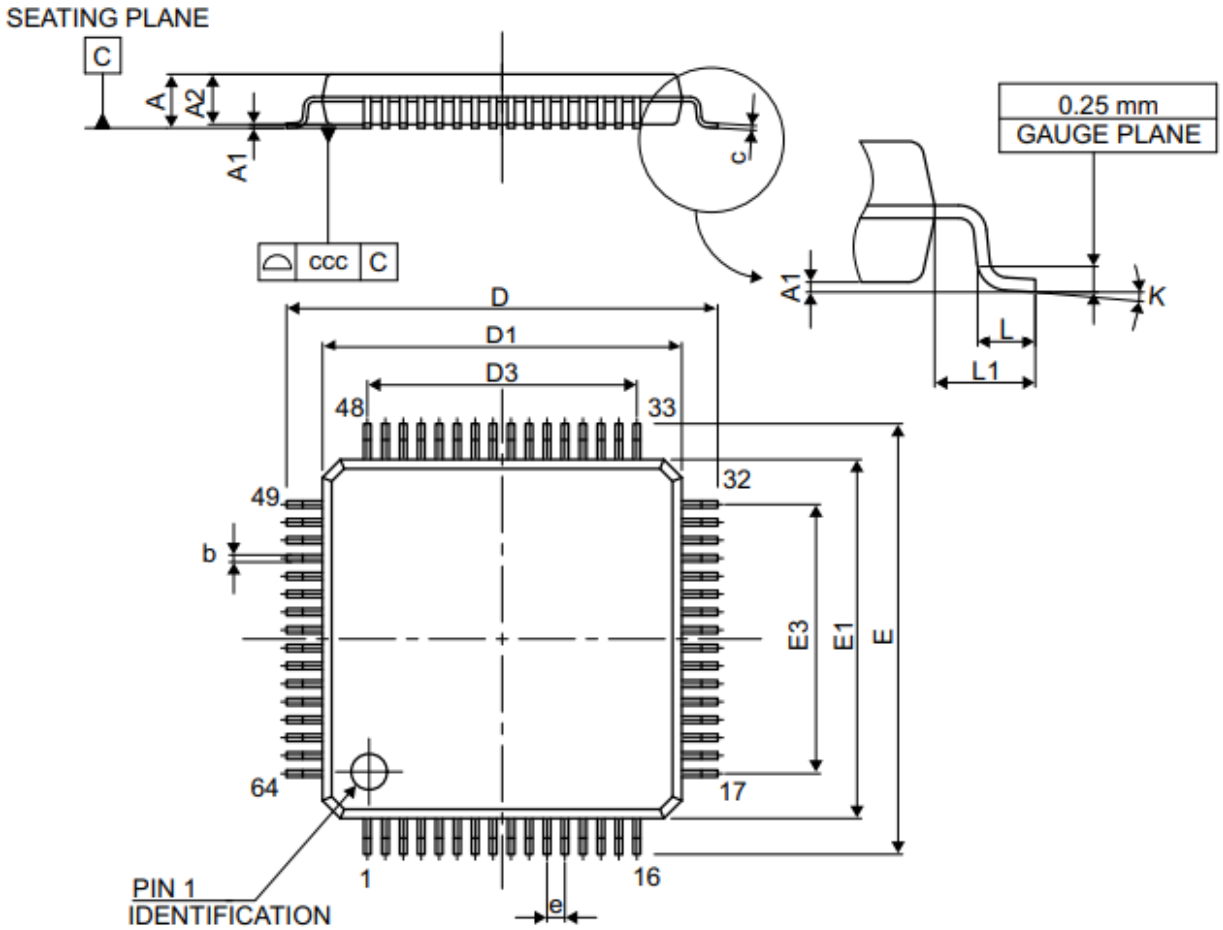
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A		0.750			0.0296	
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

7.3 LQFP64 (10x10mm) package information

LQFP64(R) is a 64-pin, 10 x 10 mm low-profile quad flat package.

LQFP64 package outline



LQFP64 package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

8 Ordering information

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest FCM sales office.

Ordering information scheme

Example: FCM32 F 072 C B T 6 - x

Device family

FCM32 = FCM 32-bit microcontroller

Product type

F = General-purpose

Sub-family

072 = FCM32x072

Pin count

K = 32 pins
C = 48 pins
R = 64 pins

User code memory size

8 = 64 Kbyte
B = 128 Kbyte

Package

T = LQFP
S = LQFP (smaller size)
U = UFQFPN

Temperature range

6 = -20 to 85℃
7 = -40 to 105℃
8 = -40 to 125℃

Options

x = Revision code

9 Revision history

Date	Revision	Author	Changes
2023/12/18	0.10	Dick Hou	Initial release
2024/9/5	0.11		Remove QFN64 package

10 Others